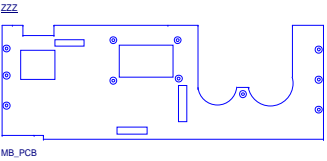


MODEL NAME : CAZ60  
PCB NO : LA-E671P  
BOM P/N : 43xxxxx



# Dell/Compal Confidential

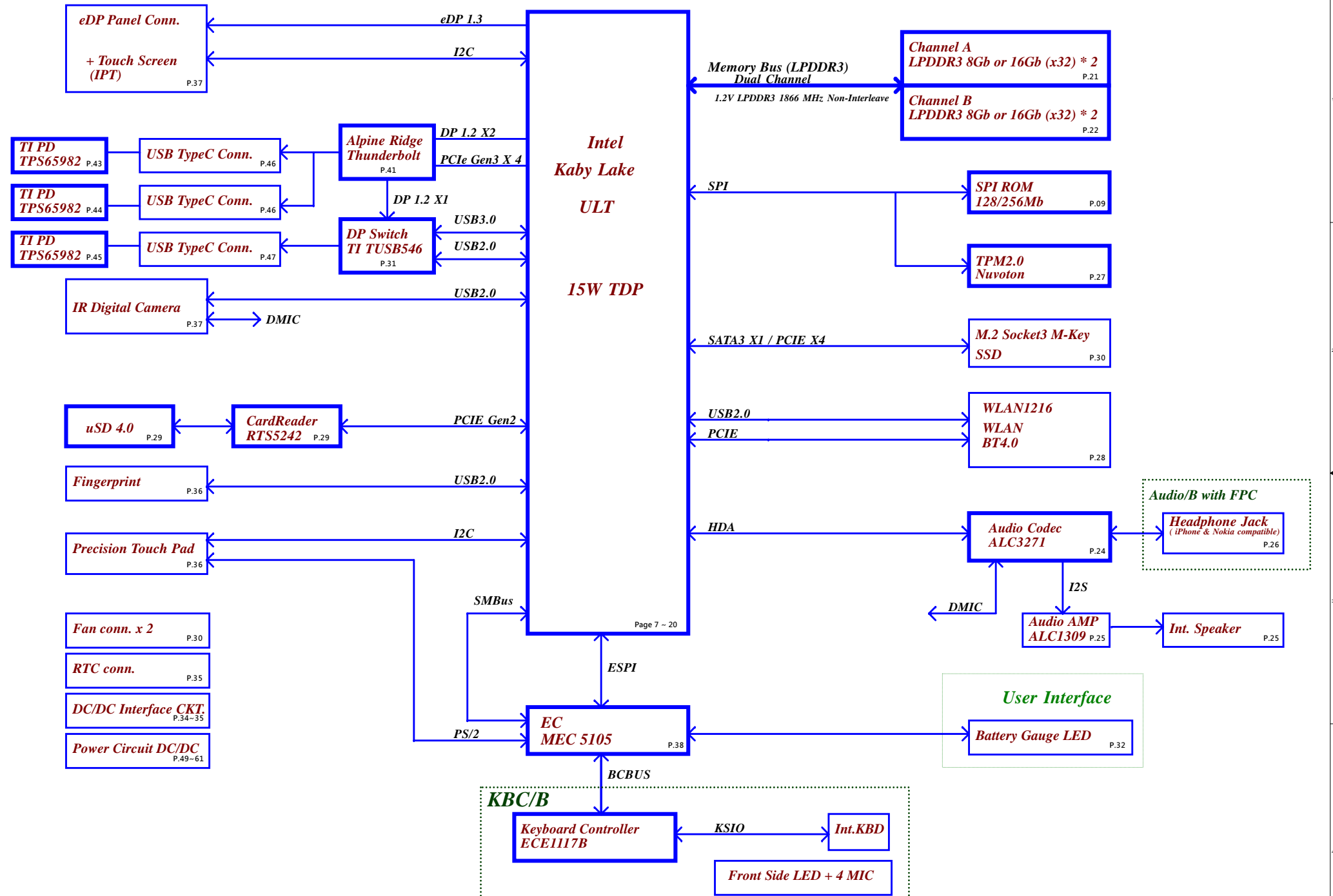
## Schematic Document

### Italia

2017-09-15

Rev: 1.0 ( A00 )

DELL CONFIDENTIAL/PROPRIETARY			
Compal Secret Data			
Title			
P01-Cover Page			
Document Number			
LA-E671P			
Rev			
1.0			
Date: Tuesday, October 17, 2017			
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### 2+2 CPU Option

UCPU1 QNB1\_2+2@  
SA0000BY0L

UCPU1 QLV1\_2+2\_R3@  
SA0000A37L

### 2+3 CPU Option

UCPU1 QMBR\_2+3\_R3@  
SA0000AH5L

### 4+2 CPU Option

UCPU1 QNEE\_4+2\_R3@  
SA0000AH5L

UCPU1 QMBF\_4+2\_R3@  
SA0000AWC2L

UCPU1 QNEF\_4+2\_R3@  
SA0000AWB3L

UCPU1 QMBE\_4+2\_R3@  
SA0000AWR2L

### AR Option

UT2 AR\_SLL42@  
SA0000R2VL  
DSL6340 SLL42 B2

### TPM Option

U7 TPM750@  
SA0000AQ200  
TPM750 - ES FW:7.1.0.0

### DRAM Option

Micron 4G/1866  
SA00009XU1L

UD41 M4G\_1866@  
SA00009XU1L

UD42 M4G\_1866@  
SA00009XU1L

UD43 M4G\_1866@  
SA00009XU1L

UD44 M4G\_1866@  
SA00009XU1L

Micron 8G/1866  
SA00009U71L

UD41 M8G\_1866@  
SA00009U71L

UD42 M8G\_1866@  
SA00009U71L

UD43 M8G\_1866@  
SA00009U71L

UD44 M8G\_1866@  
SA00009U71L

Micron 16G/1866  
SA00009ZNL

UD41 M16G\_1866@  
SA00009ZNL

UD42 M16G\_1866@  
SA00009ZNL

UD43 M16G\_1866@  
SA00009ZNL

UD44 M16G\_1866@  
SA00009ZNL

Hynix 4G/1866  
SA00008G64L

UD41 H4G\_1866@  
SA00008G64L  
H9CCNN8GTALAR-NUD

UD42 H4G\_1866@  
SA00008G64L  
H9CCNN8GTALAR-NUD

UD43 H4G\_1866@  
SA00008G64L  
H9CCNN8GTALAR-NUD

UD44 H4G\_1866@  
SA00008G64L  
H9CCNN8GTALAR-NUD

Hynix 8G/1866  
SA00008FJ4L

UD41 H8G\_1866@  
SA00008FJ4L  
H9CCNN8BTALAR-NUD

UD42 H8G\_1866@  
SA00008FJ4L  
H9CCNN8BTALAR-NUD

UD43 H8G\_1866@  
SA00008FJ4L  
H9CCNN8BTALAR-NUD

UD44 H8G\_1866@  
SA00008FJ4L  
H9CCNN8BTALAR-NUD

Hynix 16G/1866  
SA0000AEN0L

UD41 H16G\_1866@  
SA0000AEN0L  
H9CCNN16LGALAR-NUD

UD42 H16G\_1866@  
SA0000AEN0L  
H9CCNN16LGALAR-NUD

UD43 H16G\_1866@  
SA0000AEN0L  
H9CCNN16LGALAR-NUD

UD44 H16G\_1866@  
SA0000AEN0L  
H9CCNN16LGALAR-NUD

### DRAM Config Option

MEM\_CONFIG0  
RH51 M4G\_1866@  
SD028100280  
10K\_0402\_5%

MEM\_CONFIG1  
RH54 M4G\_1866@  
SD028100280  
10K\_0402\_5%

MEM\_CONFIG2  
RH56 M4G\_1866@  
SD028100280  
10K\_0402\_5%

MEM\_CONFIG3  
RH57 M4G\_1866@  
SD028100280  
10K\_0402\_5%

MEM\_CONFIG4  
RH60 M4G\_1866@  
SD028100280  
10K\_0402\_5%

RH52 M8G\_1866@  
SD028100280  
10K\_0402\_5%

RH53 M8G\_1866@  
SD028100280  
10K\_0402\_5%

RH56 M8G\_1866@  
SD028100280  
10K\_0402\_5%

RH57 M8G\_1866@  
SD028100280  
10K\_0402\_5%

RH60 M8G\_1866@  
SD028100280  
10K\_0402\_5%

RH51 M16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH53 M16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH56 M16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH57 M16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH60 M16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH52 H4G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH54 H4G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH55 H4G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH57 H4G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH60 H4G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH51 H8G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH54 H8G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH55 H8G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH57 H8G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH60 H8G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH52 H16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH53 H16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH55 H16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH57 H16G\_1866@  
SD028100280  
10K\_0402\_5%-D

RH60 H16G\_1866@  
SD028100280  
10K\_0402\_5%-D

Board ID Table for AD channel

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

CPU	4+2	2+3	3+2
Italia CAZ60			

BOARD\_ID rise ti ne is neasuredfro m5 %68 %

SMBUS Control Table

	SOURCE	BATTERY Charger	PD1	PD2	PWR_MON	5105	XDP	Audio AMP	eDP	Touch Pad	Touch S	IR_THER_S
SMB00_CLK SMB00_DATA	MEC5105			V								
SMB01_CLK SMB01_DATA	MEC5105											V
SMB02_CLK SMB02_DATA	MEC5105									V		
SMB04_CLK SMB04_DATA	MEC5105		V									
SMB05_CLK SMB05_DATA	MEC5105							V				
SMB07_CLK SMB07_DATA	MEC5105				V							
SMB10_CLK SMB10_DATA	MEC5105	V										
PCH_SML1CLK PCH_SML1DATA	PCH					V						
SMBCLK SMBDATA	PCH						V					
I2C0_CLK I2C0_DATA	PCH										V	
I2C1_CLK I2C1_DATA	PCH									V		
I2C2_CLK I2C2_DATA	PCH								V			

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Card Reader
	CLKOUT_PCIE1	NGFF WLAN	Lane 2	NC
	CLKOUT_PCIE2	NC	Lane 3	NGFF WLAN
	CLKOUT_PCIE3	M.2 SSD	Lane 4	NC
	CLKOUT_PCIE4	NC	Lane 5	Alpine Ridge
	CLKOUT_PCIE5	Card Reader	Lane 6	Alpine Ridge
	FLEX CLK#	DESTINATION	Lane 7	Alpine Ridge
	CLKOUT_LPC_0	ESPI 5105	Lane 8	Alpine Ridge
	CLKOUT_LPC_1	NC	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	NC
SATA-1A	NC
SATA-1B	NC
SATA-2	M.2 SSD

PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	PD PORT3
	2	NC
	3	NC
	4	NC
	5	IR Camera & Cam
	6	NC
	7	NGFF WLAN BT
	8	NC
	9	NC
	10	Fingerprint
PCH USB 3.0 Port Mapping	1	DP MX (PS8743B)
	2	

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

Symbol Note :

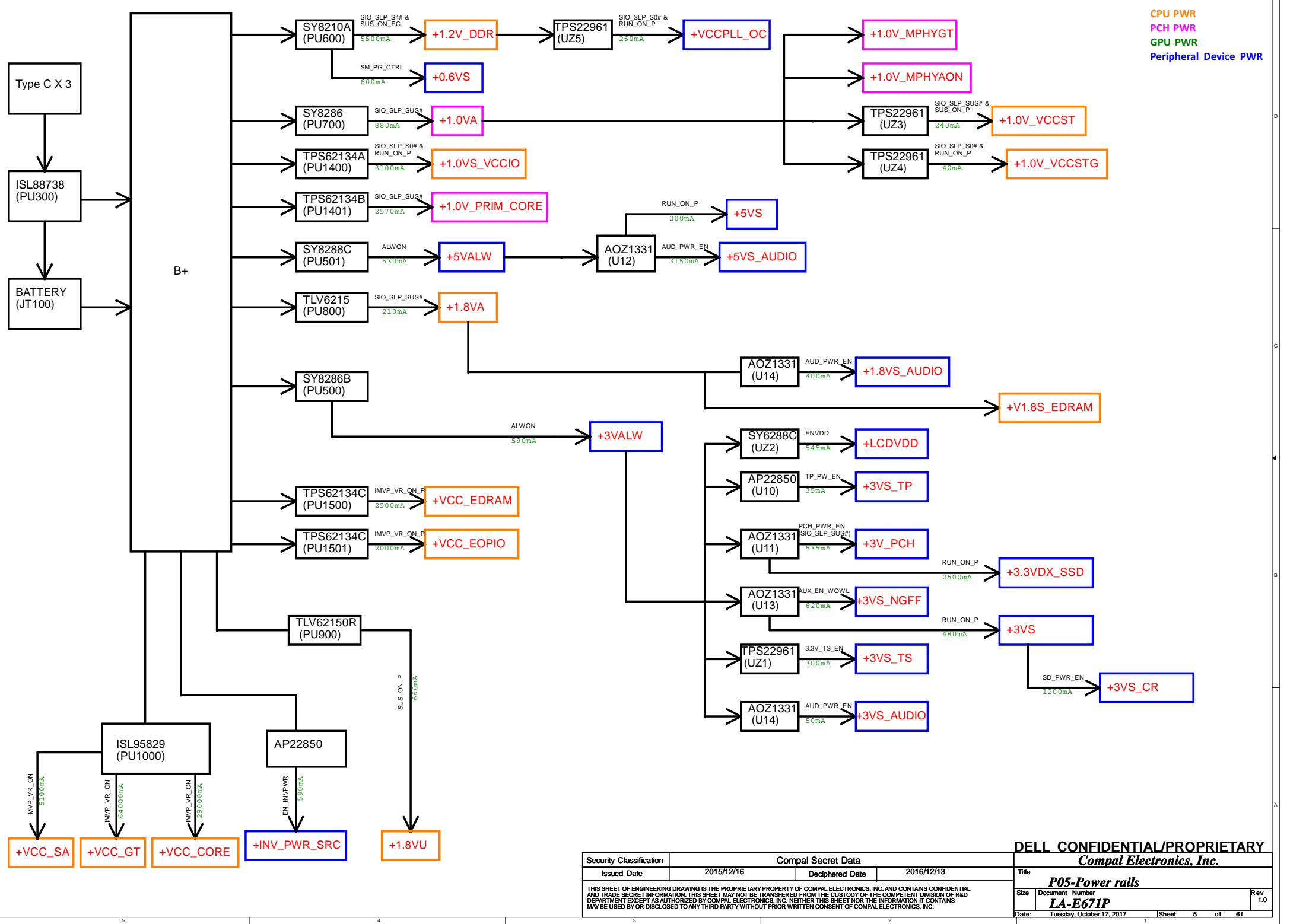


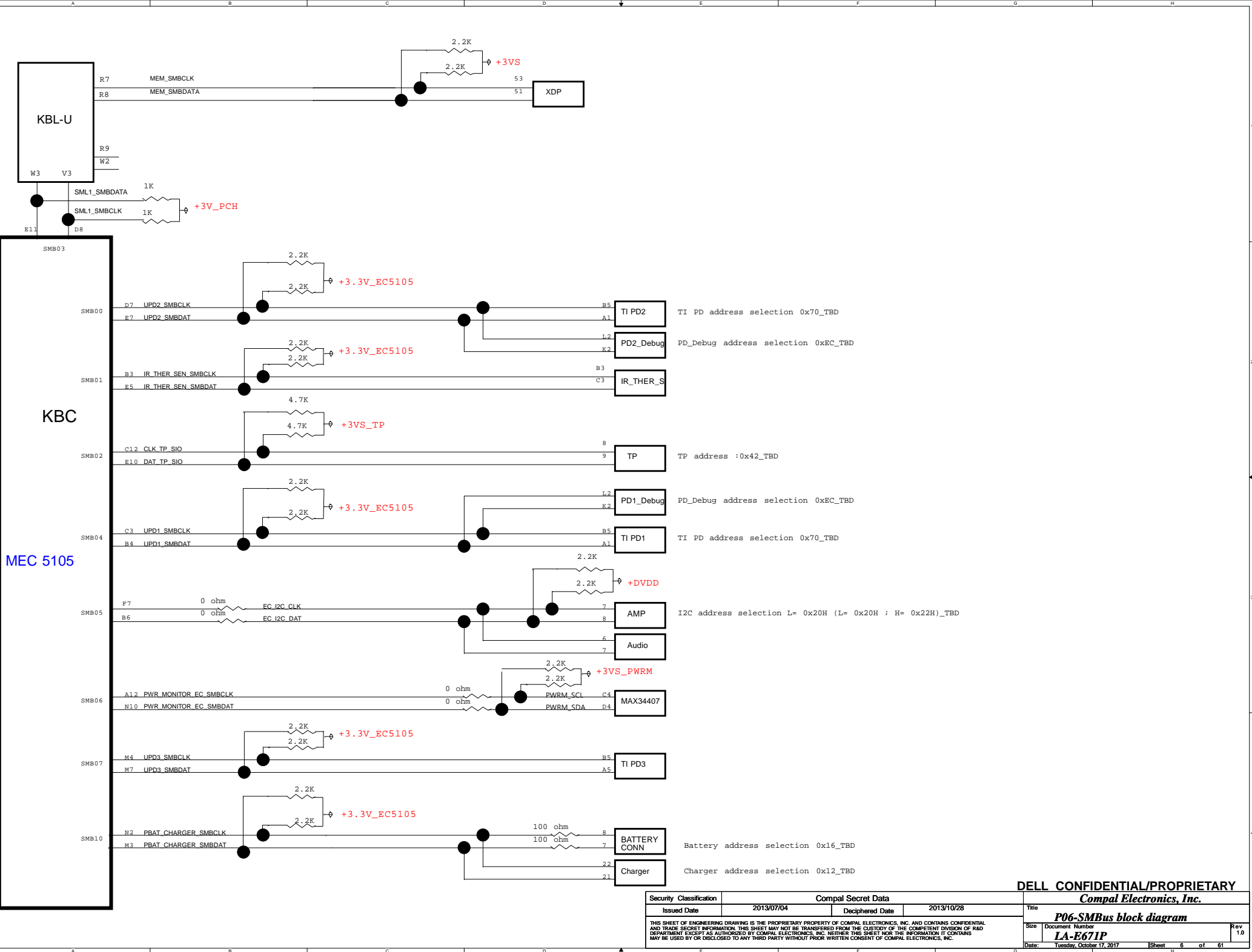
: means Digital Ground

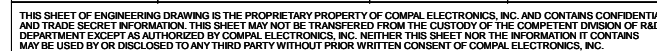


: means Analog Ground

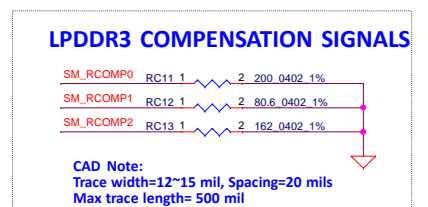
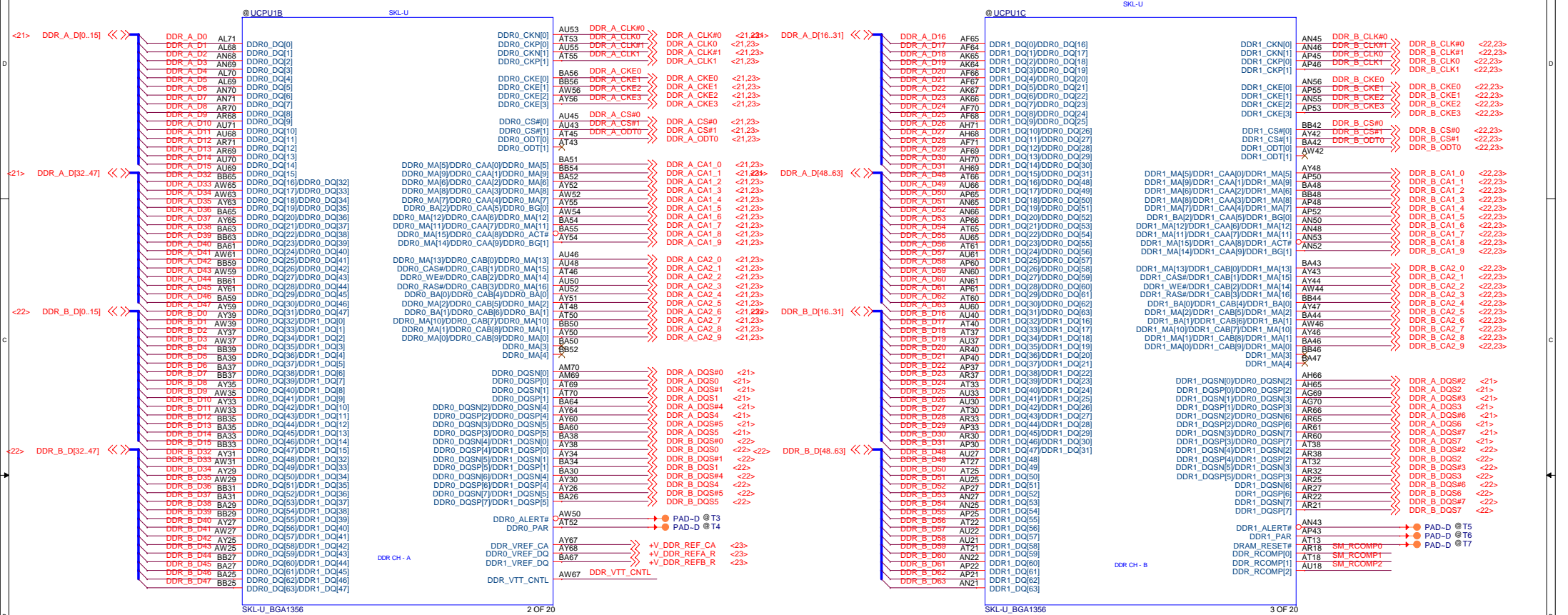
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Issued Date				2015/12/16				Compal Electronics, Inc.			
Deciphered Date				2016/12/13				P04-Notes List			
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								LA-E671P			
								Date: Tuesday, October 17, 2017			
								Sheet 4 of 61			







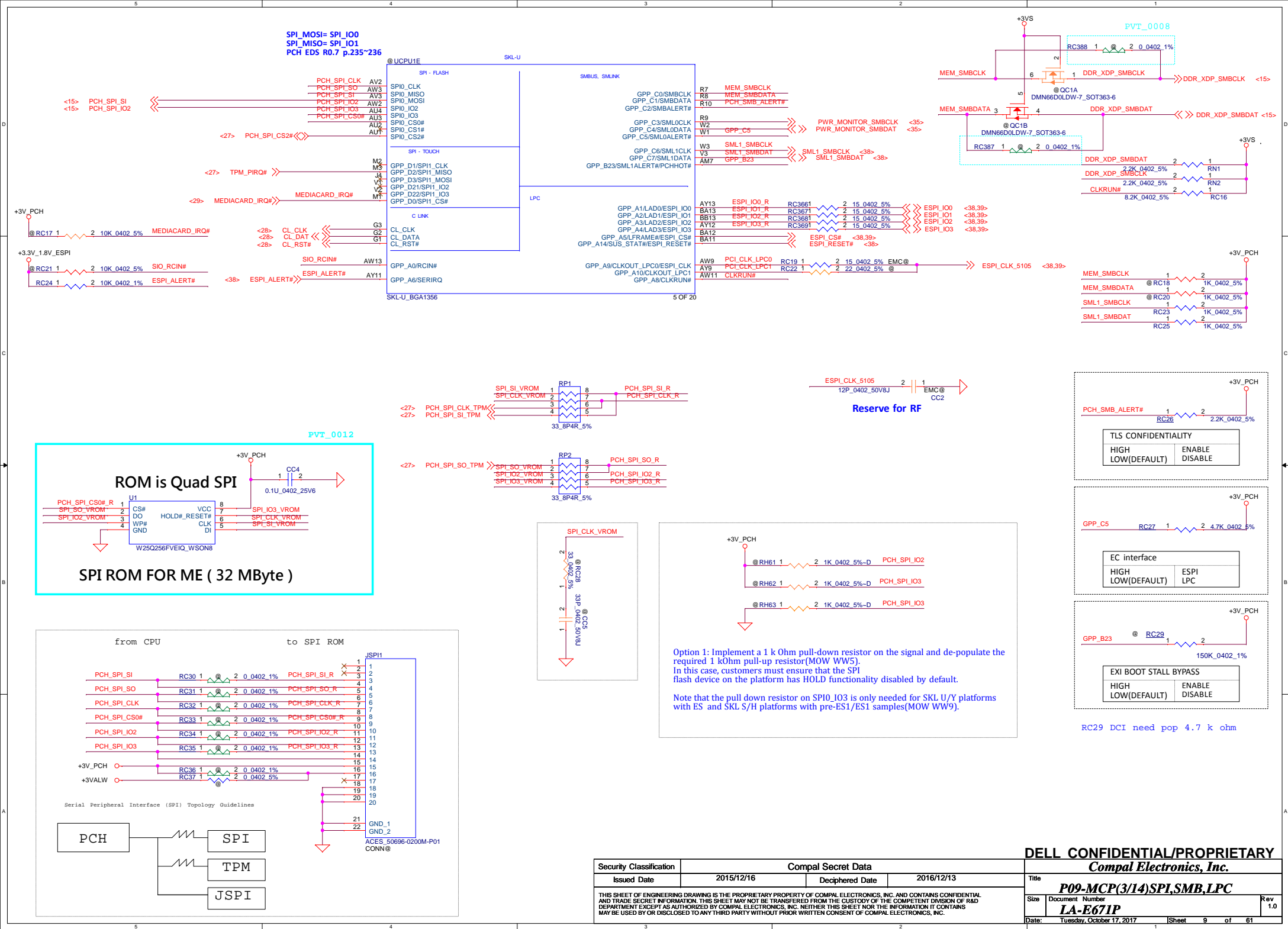
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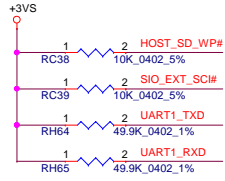


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**Compal Electronics, Inc.**

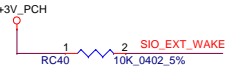
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Issued Date	2015/12/16	Deciphered Date	2016/12/13	
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Title	P08-MCP(2/14)LPDDR3			
Size	Document	Number	Rev	0.1
Date:	Tuesday, October 17, 2017	Sheet	8	of 61



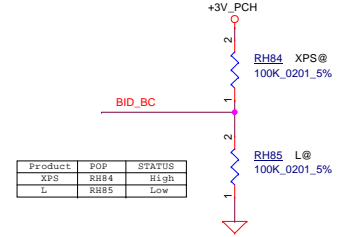
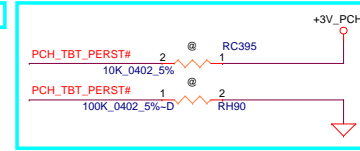
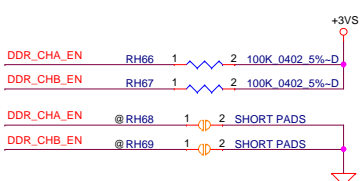
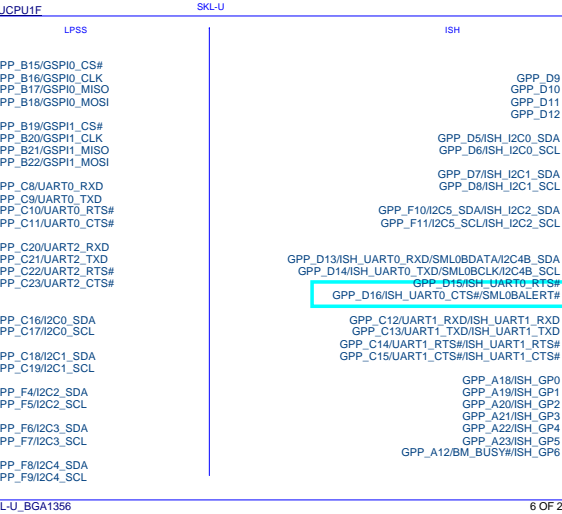
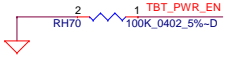




change to net name ==> I2C0\_SDA\_TS and I2C0\_SCK\_TS



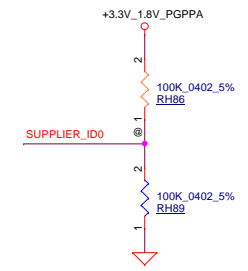
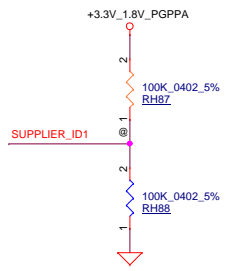
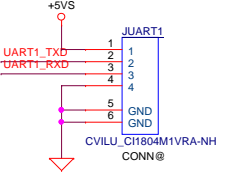
change to net name ==> I2C2\_SDA\_EDP\_PCH and I2C2\_SCK\_EDP\_PCH



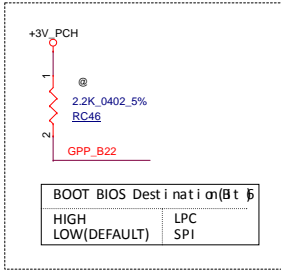
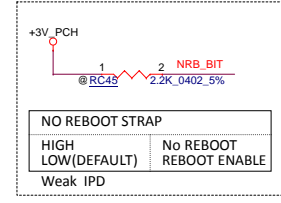
Product	POP	STATUS
XPS	RH84	High
L	RH85	Low

### TPM BOM Optional

TPM DET	
TPM	1 = W/TPM 0 = W/O TPM



RH87	RH88	RH86	RH89	REV
V	V	V	0 0	Supplier A
V	V	V	0 1	Supplier B
V	V	V	1 0	Supplier C
V	V	V	1 1	Supplier D



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Title	P10-MCP(4/14)GSPI,I2C,UART,ISH
Size	Document Number
Date	Tuesday, October 17, 2017
Sheet	10 of 61
Rev	1.0

Cardreader  
PCIe Gen2 x 1

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<29> PCIE\_PRX\_CARDTX\_P1  
<29> PCIE\_PTX\_CARDRX\_N1  
<29> PCIE\_PTX\_CARDRX\_P1

WLAN  
PCIe Gen2 x 1

<28> PCIE\_PRX\_WLANTX\_N3  
<28> PCIE\_PRX\_WLANTX\_P3  
<28> PCIE\_PTX\_WLANRX\_N3  
<28> PCIE\_PTX\_WLANRX\_P3

Alpine Ridge  
PCIe Gen3 x 4

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<41> PCIE\_PTX\_TBRX\_N5  
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M.2 SSD  
PCIe Gen3 x 4

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SATA SSD

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<30> SATA\_PTX\_SSDRX\_N2  
<30> SATA\_PTX\_SSDRX\_P2

@UCPU1H

SKL-U

PCIe/USB3/SATA

SSIC / USB3

H13 PCIE1\_RXN/USB3\_5\_RXN  
G13 PCIE1\_RXP/USB3\_5\_RXP  
B17 PCIE1\_TXN/USB3\_5\_TXN  
A17 PCIE1\_TXP/USB3\_5\_TXP  
  
G11 PCIE2\_RXN/USB3\_6\_RXN  
F11 PCIE2\_RXP/USB3\_6\_RXP  
D18 PCIE2\_TXN/USB3\_6\_TXN  
C18 PCIE2\_TXP/USB3\_6\_TXP  
  
H16 PCIE3\_RXN  
G16 PCIE3\_RXP  
D17 PCIE3\_TXN  
C17 PCIE3\_TXP  
  
G15 PCIE4\_RXN  
F15 PCIE4\_RXP  
B19 PCIE4\_TXN  
A19 PCIE4\_TXP  
  
F16 PCIE5\_RXN  
E16 PCIE5\_RXP  
C19 PCIE5\_TXN  
D19 PCIE5\_TXP  
  
G18 PCIE6\_RXN  
F18 PCIE6\_RXP  
D20 PCIE6\_TXN  
C20 PCIE6\_TXP  
  
F20 PCIE7\_RXN/SATA0\_RXN  
E20 PCIE7\_RXP/SATA0\_RXP  
B21 PCIE7\_TXN/SATA0\_TXN  
A21 PCIE7\_TXP/SATA0\_TXP  
  
G21 PCIE8\_RXN/SATA1A\_RXN  
F21 PCIE8\_RXP/SATA1A\_RXP  
D21 PCIE8\_TXN/SATA1A\_TXN  
C21 PCIE8\_TXP/SATA1A\_TXP  
  
E22 PCIE9\_RXN  
D22 PCIE9\_RXP  
B23 PCIE9\_TXN  
A23 PCIE9\_TXP  
  
F25 PCIE10\_RXN  
E25 PCIE10\_RXP  
D23 PCIE10\_TXN  
C23 PCIE10\_TXP  
  
F5 PCIE\_RCOMP\_N  
E5 PCIE\_RCOMP\_P  
  
D56 PROC\_PRDY#  
BB11 PROC\_PREQ#  
X GPP\_A7PIRQA#  
  
E28 PCIE11\_RXN/SATA1B\_RXN  
D27 PCIE11\_RXP/SATA1B\_RXP  
D24 PCIE11\_TXN/SATA1B\_TXN  
C24 PCIE11\_TXP/SATA1B\_TXP  
  
E30 PCIE12\_RXN/SATA2\_RXN  
D25 PCIE12\_RXP/SATA2\_RXP  
B25 PCIE12\_TXN/SATA2\_TXN  
A25 PCIE12\_TXP/SATA2\_TXP

USB3\_1\_RXN H8  
USB3\_1\_RXP G8  
USB3\_1\_TXN C13  
USB3\_1\_TXP D13  
  
USB3\_2\_RXN/SSIC\_1\_RXN J6  
USB3\_2\_RXP/SSIC\_1\_RXP H6  
USB3\_2\_TXN/SSIC\_1\_TXN B13  
USB3\_2\_TXP/SSIC\_1\_TXP A13  
  
USB3\_3\_RXN/SSIC\_2\_RXN J10  
USB3\_3\_RXP/SSIC\_2\_RXP H10  
USB3\_3\_TXN/SSIC\_2\_TXN B15  
USB3\_3\_TXP/SSIC\_2\_TXP A15  
  
USB3\_4\_RXN E10  
USB3\_4\_RXP C10  
USB3\_4\_TXN C15  
USB3\_4\_TXP D15  
  
USB2N\_1 AB9  
USB2P\_1 AB10  
  
USB2N\_2 AD6  
USB2P\_2 AD7  
  
USB2N\_3 AH3  
USB2P\_3 AJ3  
  
USB2N\_4 AD9  
USB2P\_4 AD10  
  
USB2N\_5 AJ1  
USB2P\_5 AJ2  
  
USB2N\_6 AF6  
USB2P\_6 AF7  
  
USB2N\_7 AH1  
USB2P\_7 AH2  
  
USB2N\_8 AF8  
USB2P\_8 AF9  
  
USB2N\_9 AG1  
USB2P\_9 AG2  
  
USB2N\_10 AH7  
USB2P\_10 AH8  
  
USB2N\_COMP AB6  
USB2P\_COMP AG3  
USB2\_ID RC48  
USB2\_VBUSSENSE AG4  
VBUSSENSE RC49  
  
GPP\_E9/USB2\_OC0# C9  
GPP\_E10/USB2\_OC1# D9  
GPP\_E11/USB2\_OC2# B9  
GPP\_E12/USB2\_OC3# B9  
  
GPP\_E4/DEVSLP# J1  
GPP\_E5/DEVSLP# J2  
GPP\_E6/DEVSLP# J3  
  
GPP\_E0/SATA0PCIE0/SATAGP0 H2  
GPP\_E1/SATA0PCIE1/SATAGP1 H3  
GPP\_E2/SATA0PCIE2/SATAGP2 H4  
GPP\_E8/SATA0PCIE8/SATAGP8 H1  
  
TBT\_A\_USB\_OC0# A8  
TBT\_B\_USB\_OC1# C9  
MUX\_C\_USB\_OC2# D9  
USB\_OC3# B9  
  
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SSD\_IFDET <30>

USB3.0 DP MX (PS8743B)

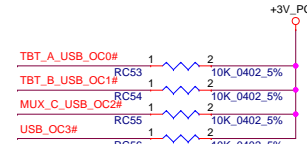
USB2.0 for USB PD PORT3

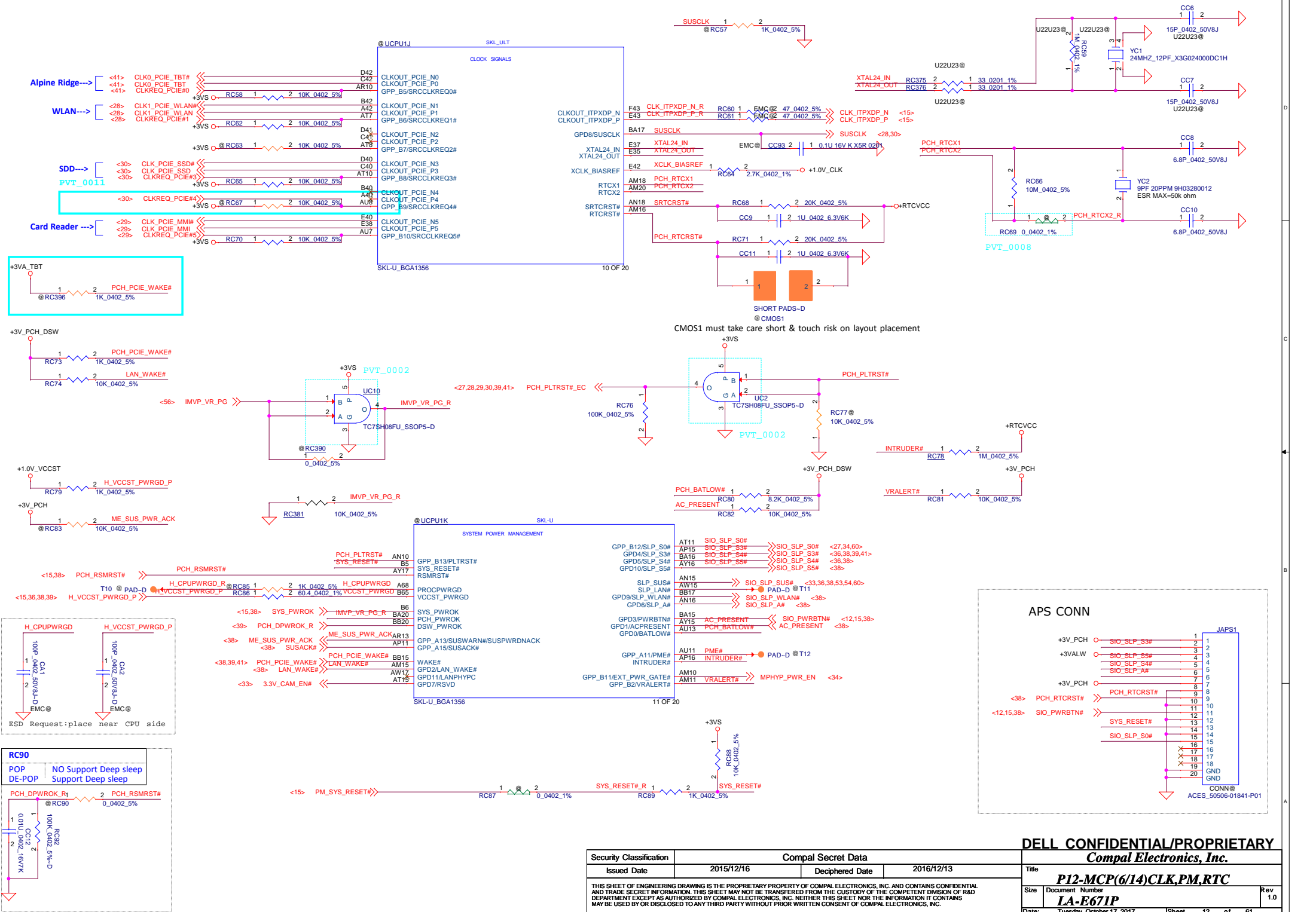
CAM & IR CAM

NGFF (WLAN)

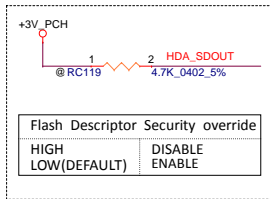
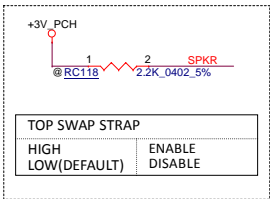
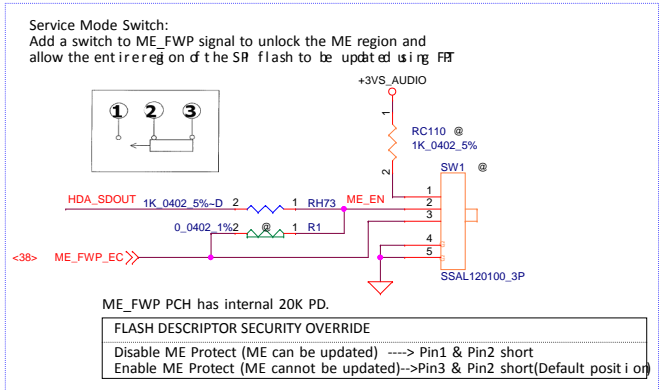
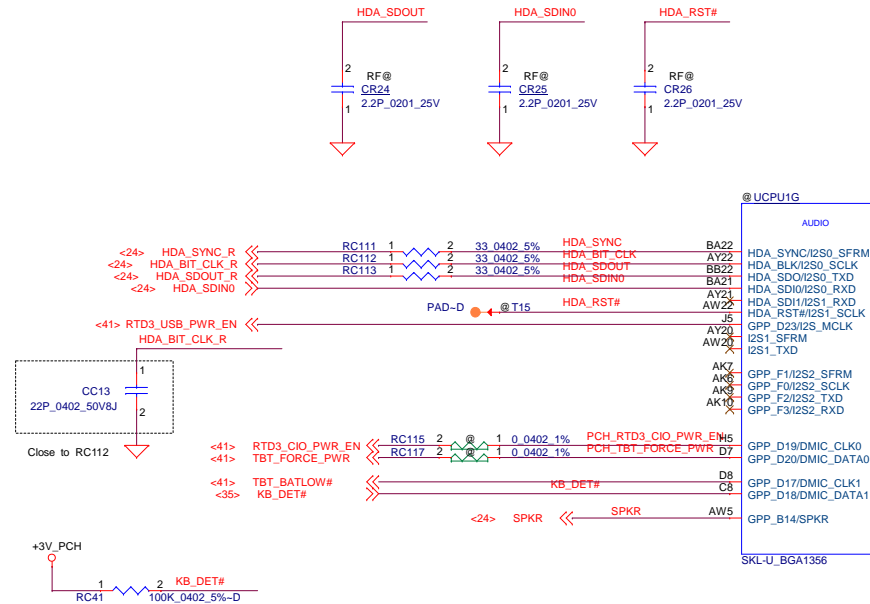
Fingerprint

PVT\_0008

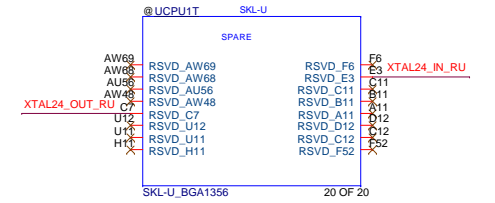
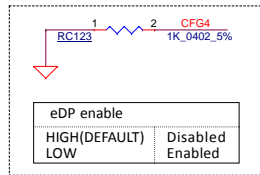
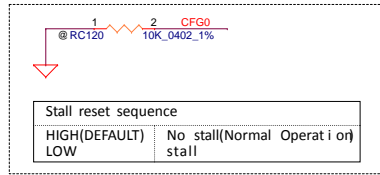




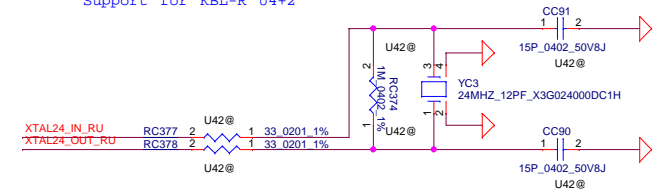
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Title P12-MCP(6/14)CLK,PM,RTC			
Size LA-E671P		Document Number Rev 1.0	
Date: Tuesday, October 17, 2017		Sheet 12 of 61	



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Title P13-MCP(7/14)MISC,JTAG,HDA,SDIO			
Size	Document Number LA-E671P		Rev 1.0
Date:	Tuesday, October 17, 2017	Sheet 13	of 61

[illegible]

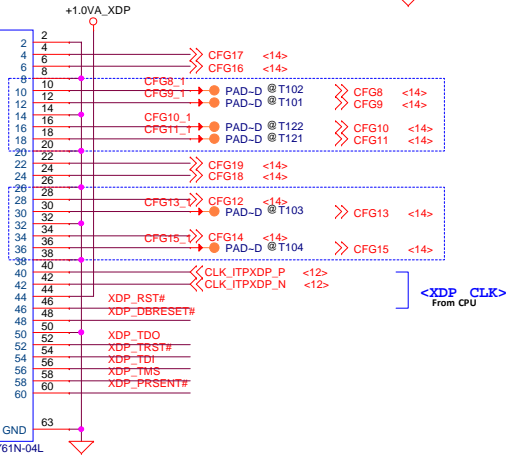
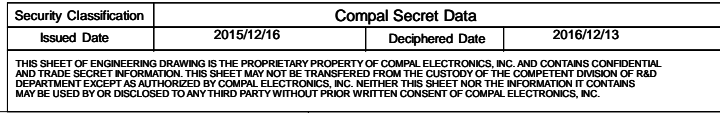
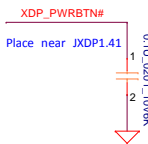
Support for KBL-R U4+2



ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

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Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title	<b>P14-MCP(8/14)CFG.RSVD</b>	
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				<b>LA-E671P</b>		
				Date:	Tuesday, October 17, 2017	Sheet 14 of 61



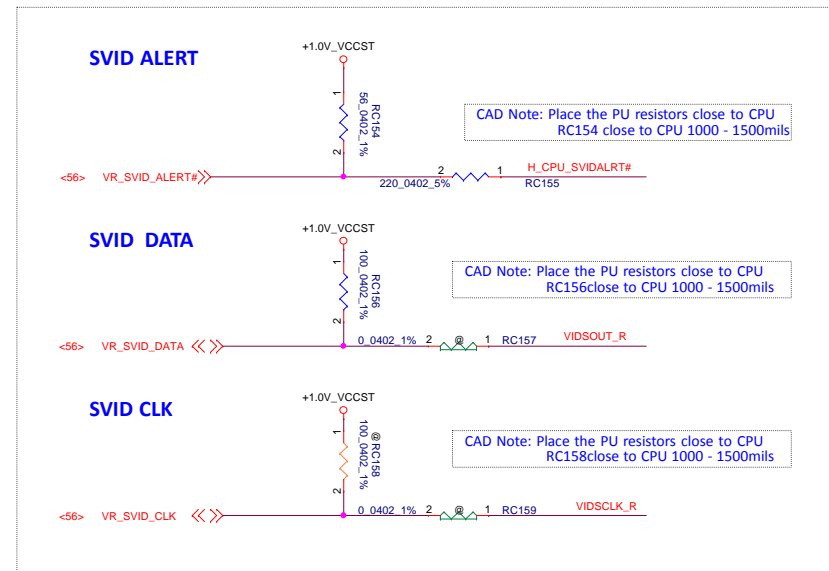
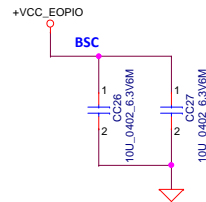
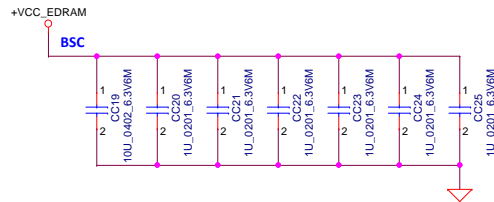
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Size	Document Number	Rev	
	<b>LA-E671P</b>	1.0	
Date:	Tuesday, October 17, 2017	Sheet	15 of 61



**Component placement order:**  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

[illegible]

+VCC\_EOPIO Decoupling Requirment  
Back Side (underneath the package):  
10U\_0402\*2 pcs



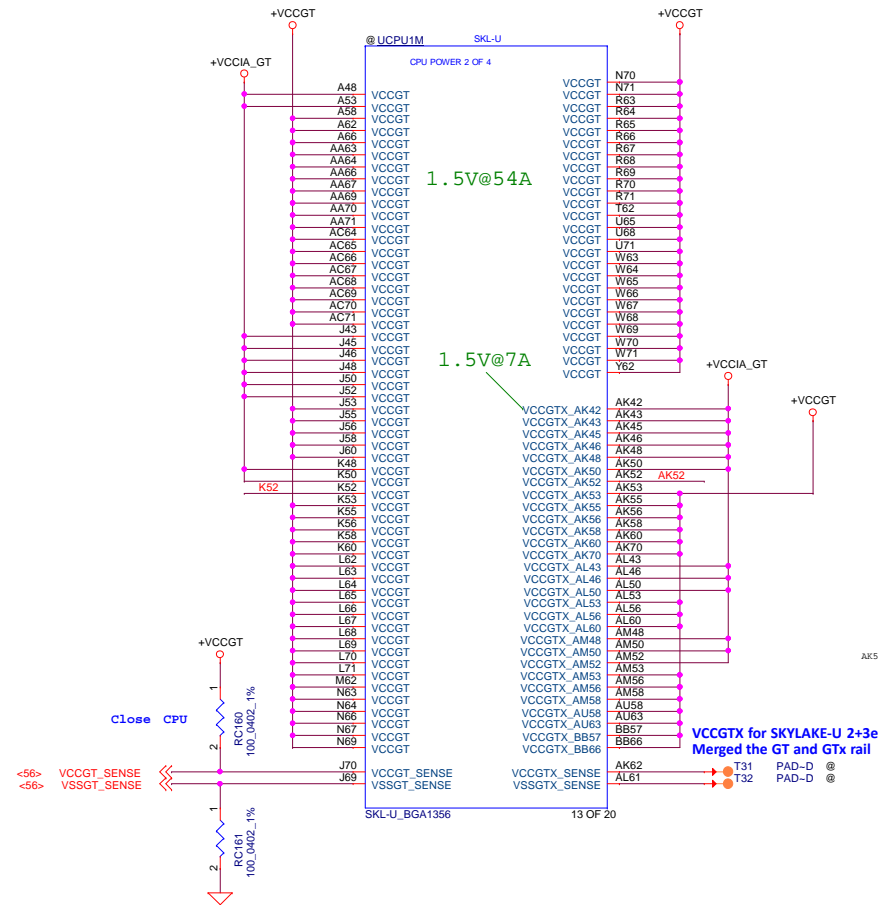
**Compal Electronics, Inc.**

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Issued Date		2015/12/16	Deciphered Date		2016/12/13	Title <b>P16-MCP(10/14)PWR-VCC CORE</b>		
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						Date: Tuesday, October 17, 2017		
						<b>LA-E671P</b>		

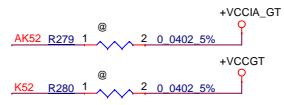
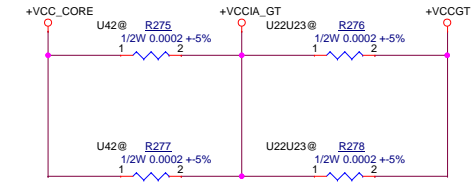
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+VCCGT: 0.55~1.5V, 54A  
+VCCGTx : 0.55~1.5V, 7A



Note: 4+2 Co-layout Only can use SD00001V200



KBL-R U42 Only Design	Do not Connect AK52 and K52 Balls, Keep as NC
KBL-R U42 Compatible Design for (KBL-R U42/KBL U22/KBL U23e) support	Do not Connect AK52 and K52 Balls, Keep as NC

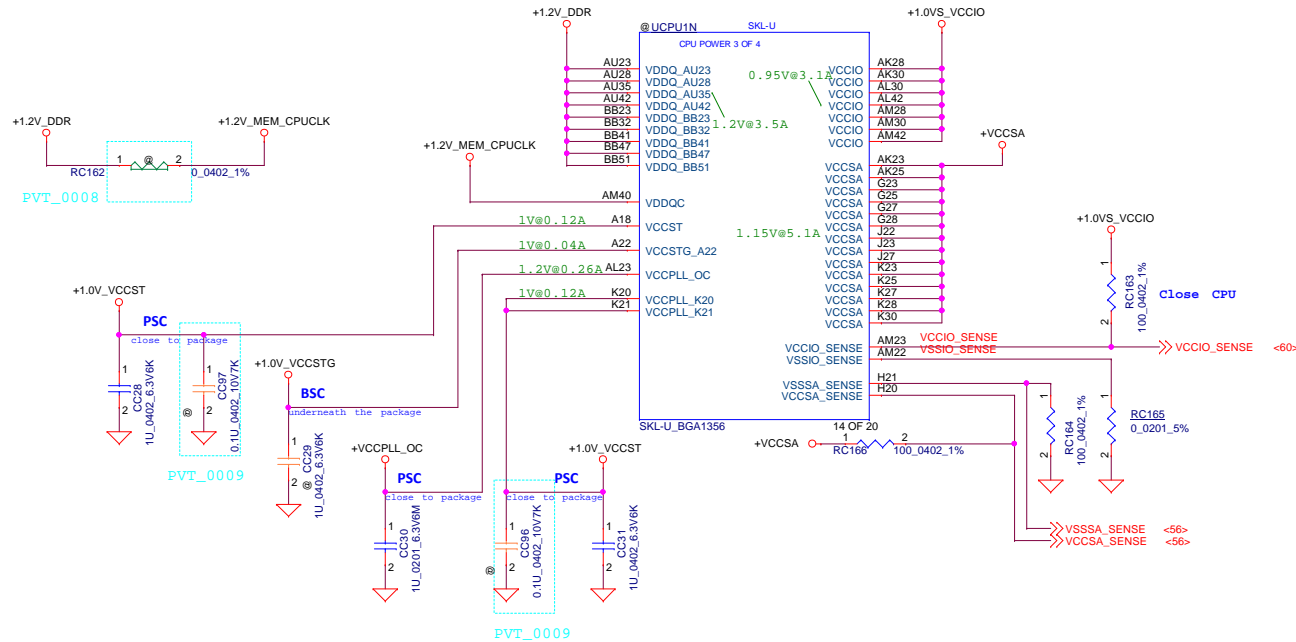
AK52 and K52 Kaby Lake Silicon Ball Connectivity Recap from PDG (568813\_KBL\_R\_U42\_PDG\_Addendum\_Rev0p9, Page 12)

VCCGTx for SKYLAKE-U 2+3e  
Merged the GT and GTx rail

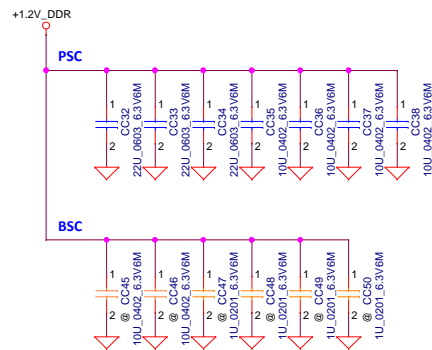
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				LA-E671P
				Rev 1.0
				Date: Tuesday, October 17, 2017
				Sheet 17 of 61

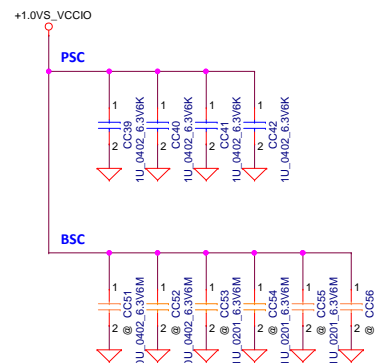
**+1.2V\_DDR: 1.2V, 3.5A**  
**+1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA**  
**+1.0V\_VCCSTG: 1V, 40mA**  
**+VCCPLL\_OC: 1.2V, 260mA**  
**+1.0VS\_VCCIO: 0.85~0.95V, 3.1A**  
**+VCC\_SA: 1.15V, 5.1A**



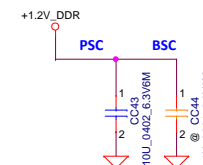
**+1.2\_DDR Decoupling Requirement**  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (@)  
 Primary Side (close to package):  
 10U\_0402\*4 pcs + 22U\_0603\*3 pcs



**+1.0VS\_VCCIO Decoupling Requirement**  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (@)  
 Primary Side (close to package):  
 1U\_0402\*4 pcs



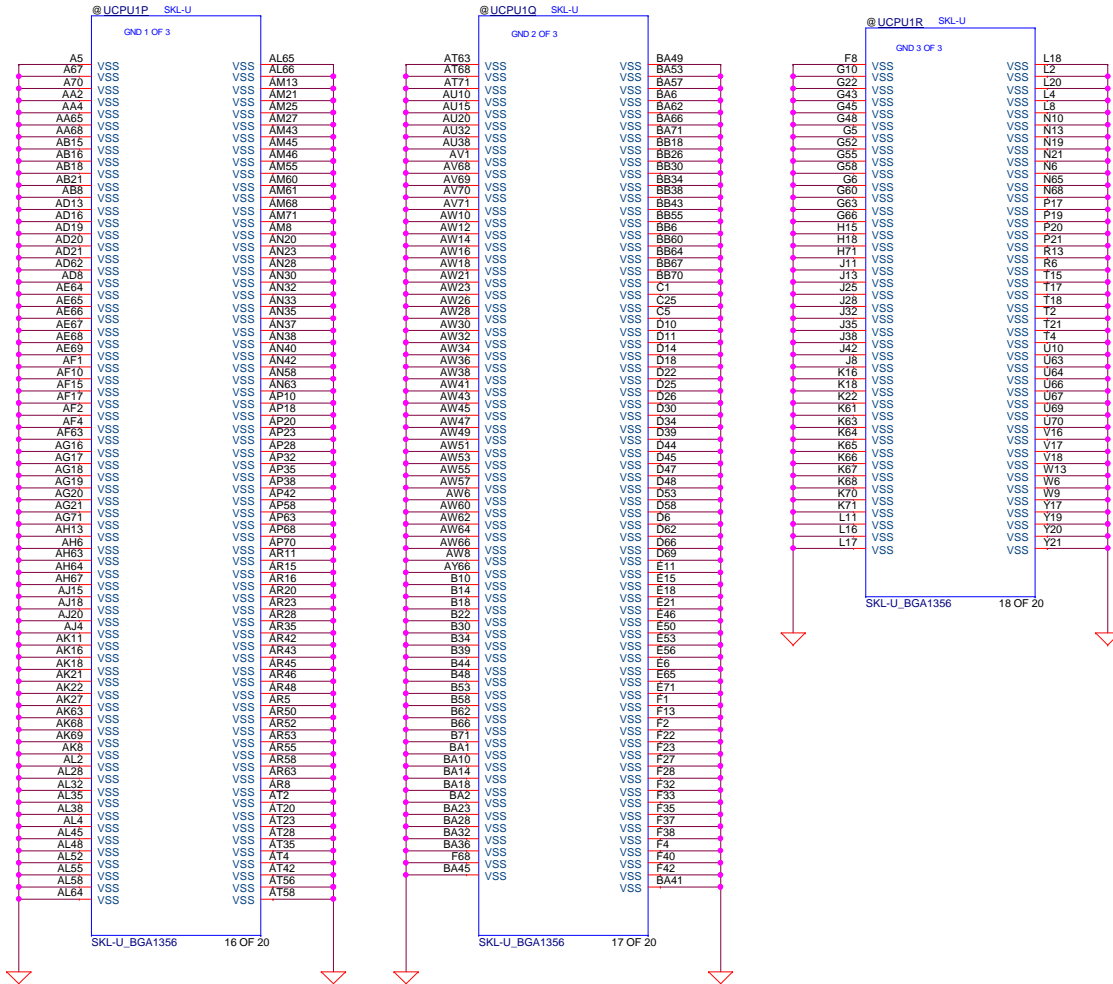
**+1.2V\_MEM\_CPUCLK (VDDQC) Place on CPU**  
 Back Side (underneath the package):  
 1U\_0201\*1 pcs (@)  
 Primary Side (close to package):  
 10U\_0402 \* 1 pcs



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Deciphered Date				2016/12/13				Title			
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				LA-E671P				Document Number			
				Rev 1.0				Date: Tuesday, October 17, 2017			
								Sheet 18 of 61			



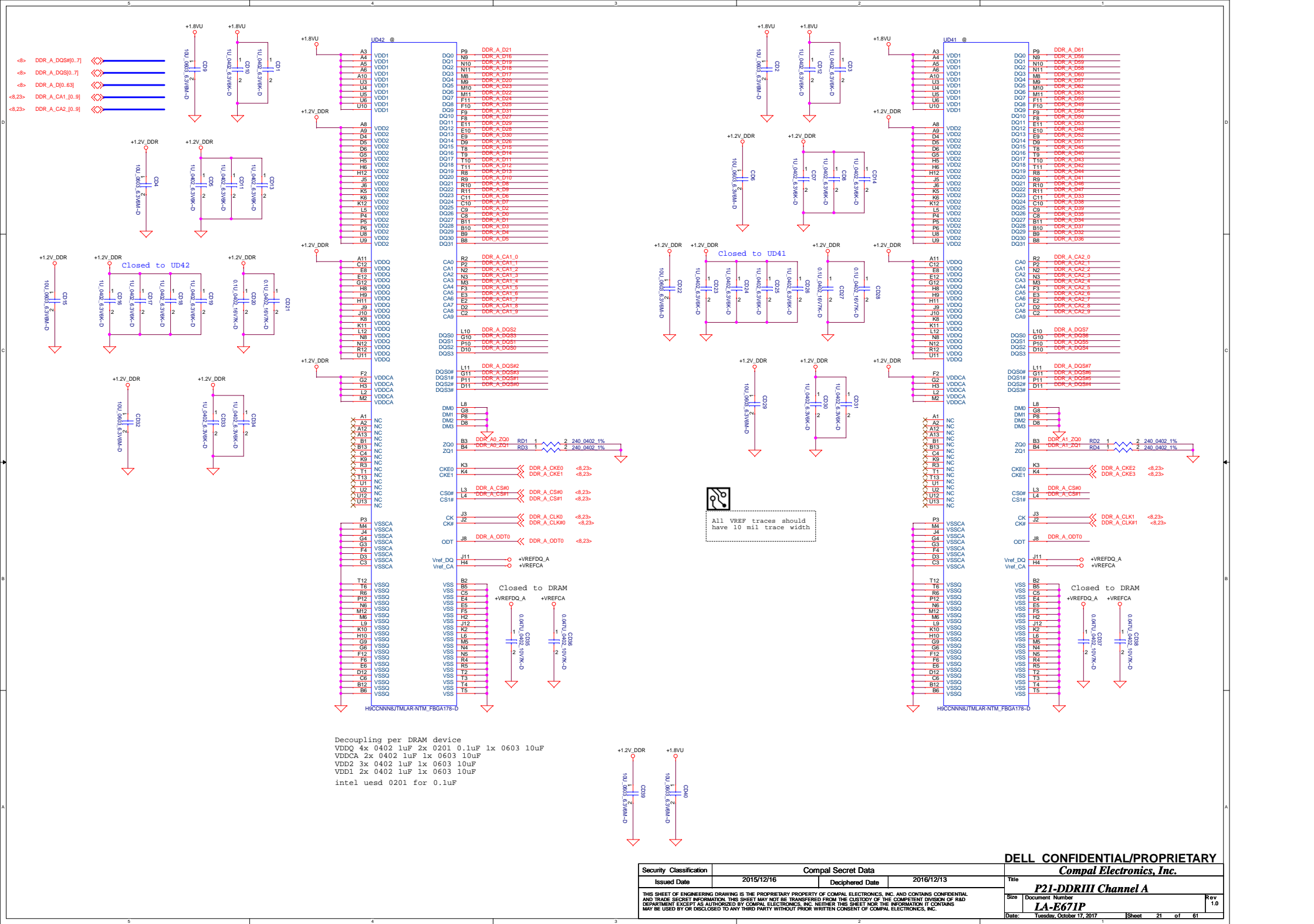
Note1: VCCPRIM\_CORE Implementat i on uñt h PCH CORE\_V D Reco mnendat i on



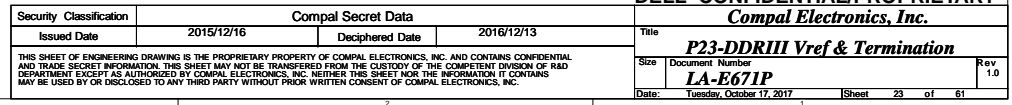
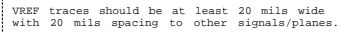
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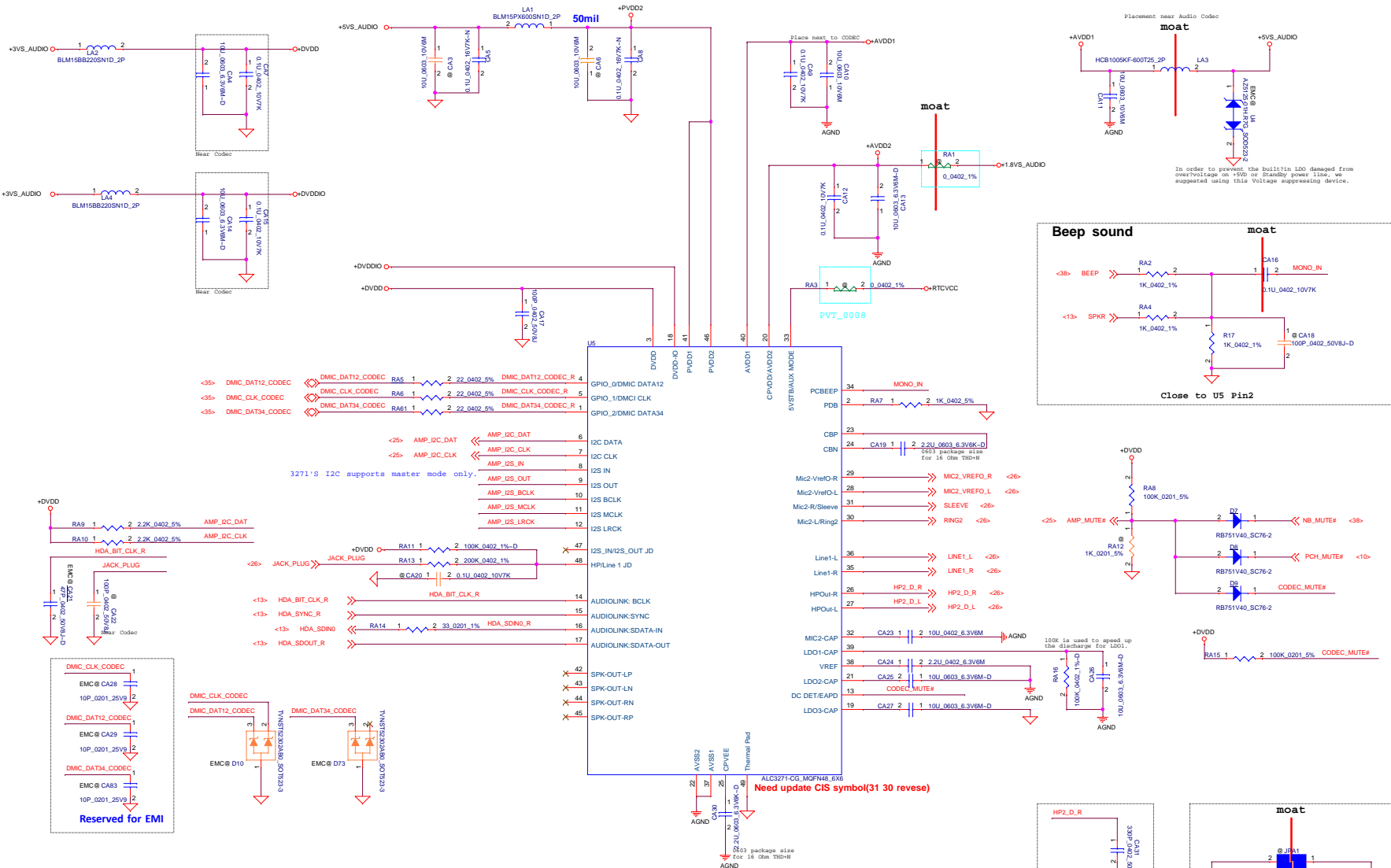
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Issued Date	2015/12/16	Deciphered Date	2016/12/13	P20-MCP(14/14)VSS	
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				LA-E671P	Rev 1.0
				Date: Tuesday, October 17, 2017	Sheet 20 of 61



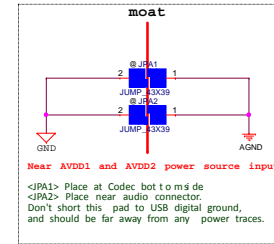
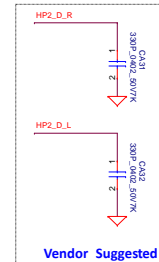
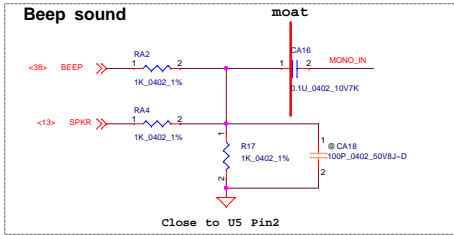
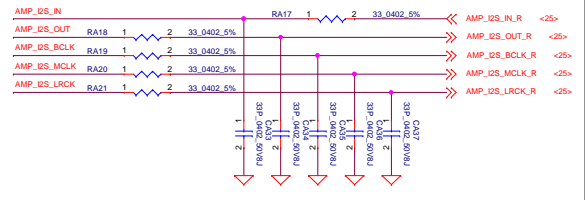




# HD Audio Codec



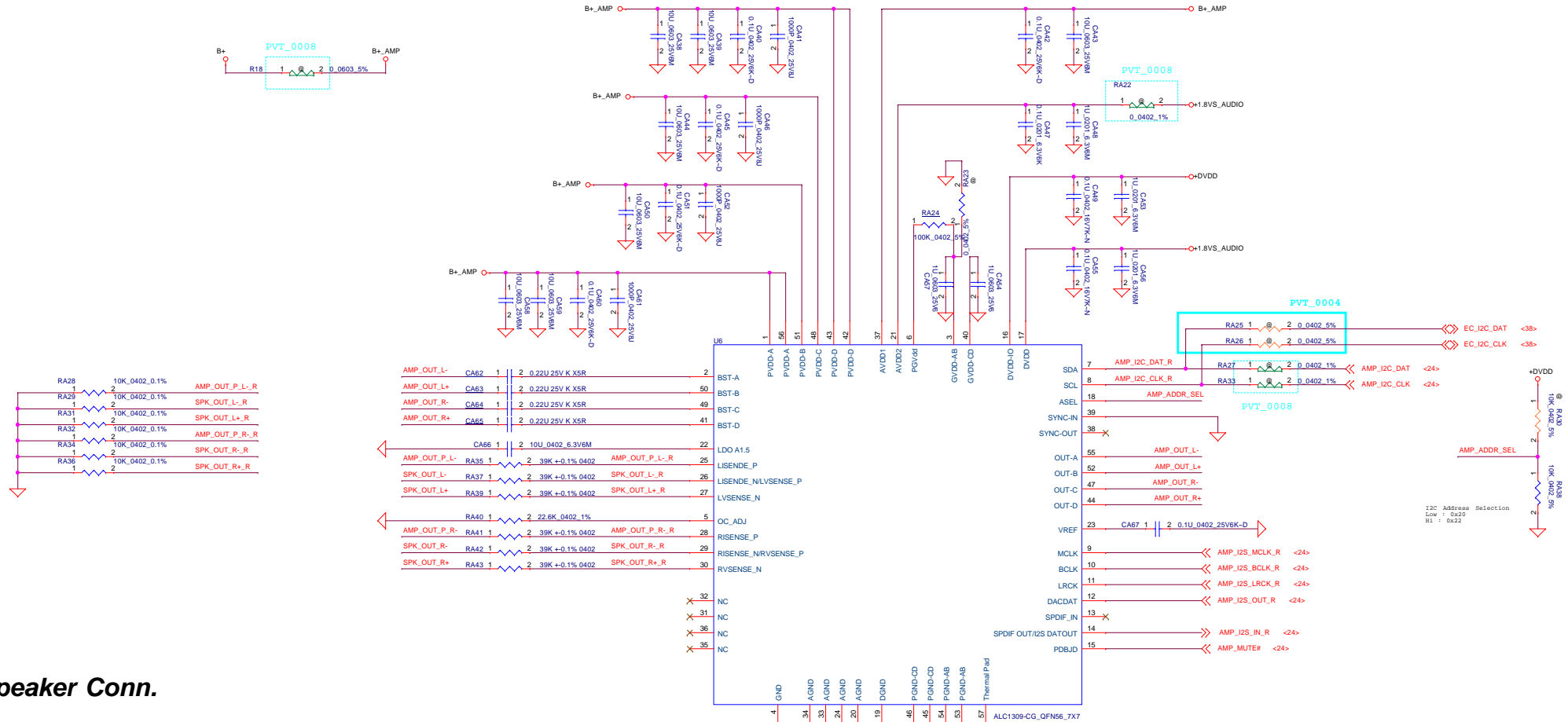
## POST I2S interface



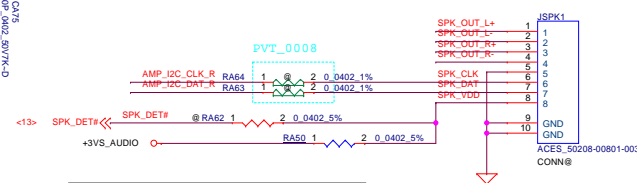
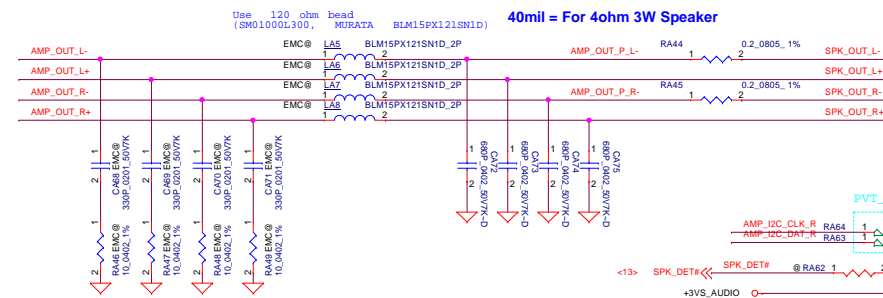
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Issued Date		Deciphered Date		Title	
2013/07/04		2013/10/28		P24-Audio Codec3271	
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				Rev 1.0	
Date:		Tuesday, October 17, 2017		Sheet 24 of 61	



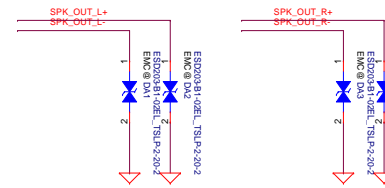
## SMART AMP



**Int. Speaker Conn.**

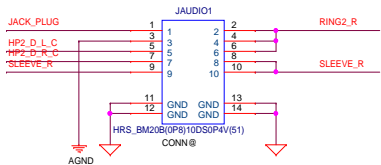
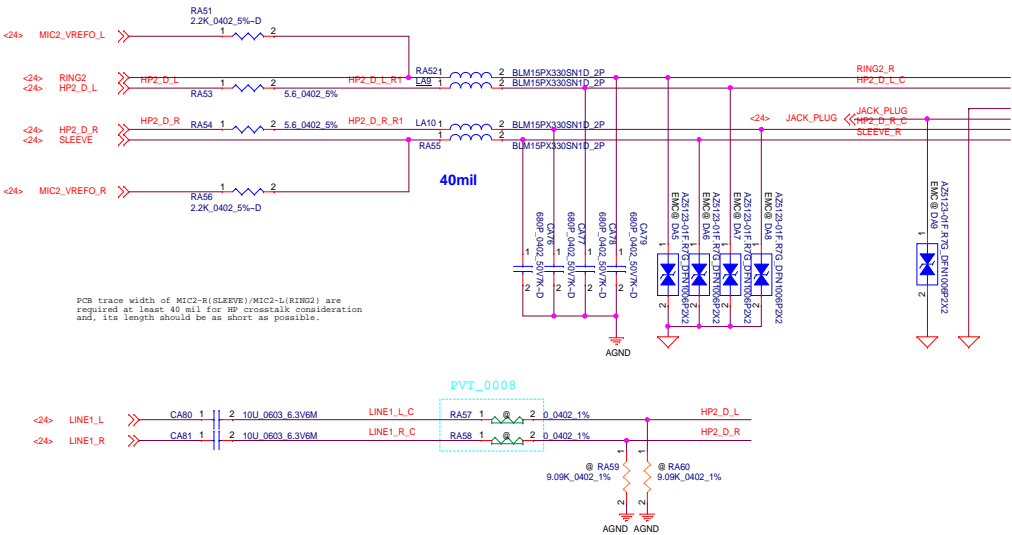


Function	RA50	RA62
EEPROM Speaker	0 ohm	NC
Speaker Detection	10K	0 ohm



Security Classification	Compal Secret Data			Title		
Issued Date	2014/09/08	Deciphered Date	2013/10/28	P25-Smart AMP / Speaker		
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Universal Audio Jack

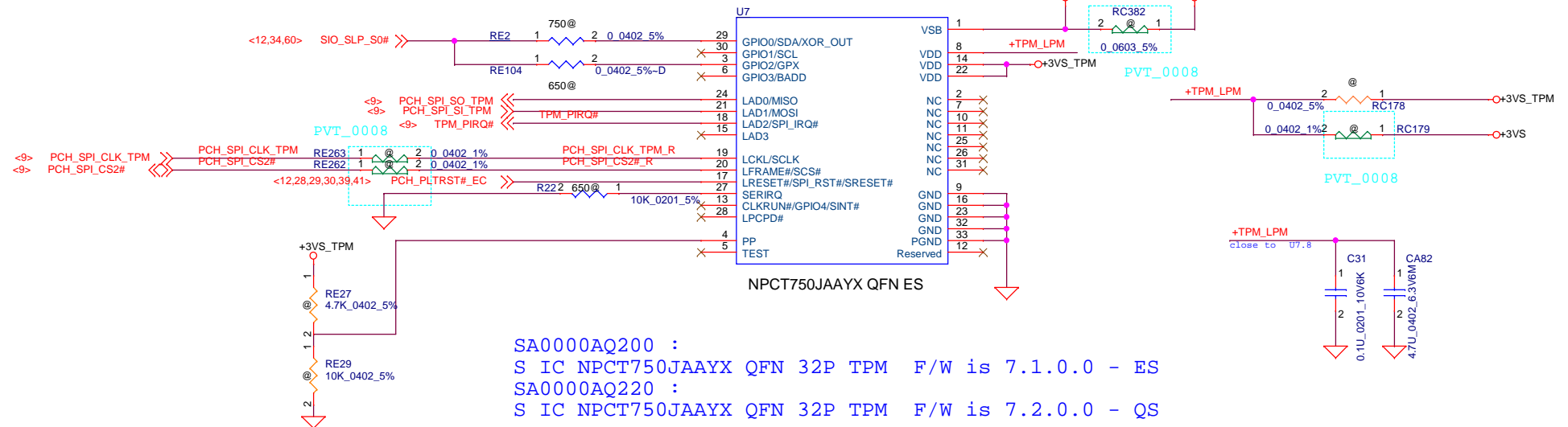
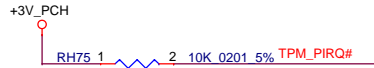
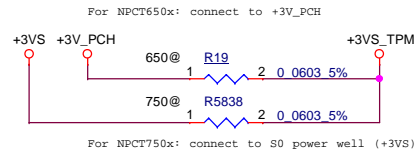


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Deciphered Date				2013/10/28				Title			
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								Document Number			
								LA-E671P			
								Rev			
								1.0			
								Date: Tuesday, October 17, 2017			
								Sheet 26 of 61			

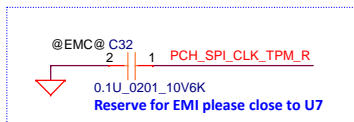
NOTE:  
Follow the SPI topology layout guidelines  
in the relevant Intel Platform Design Guide

# TPM

NOTE:  
Place 0.1 uF capacitors as close as  
possible to the device power pins



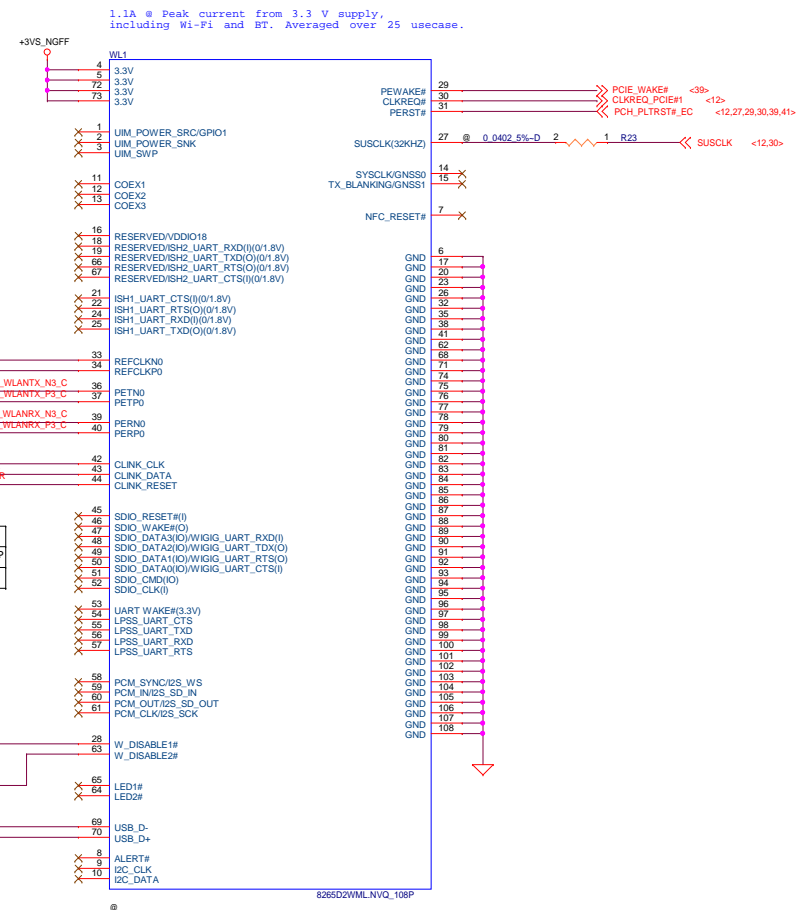
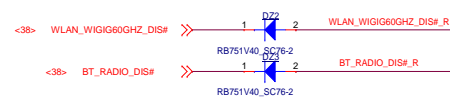
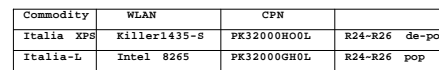
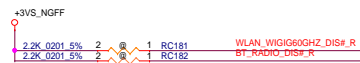
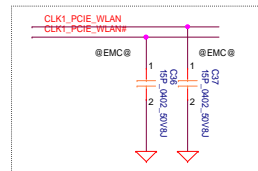
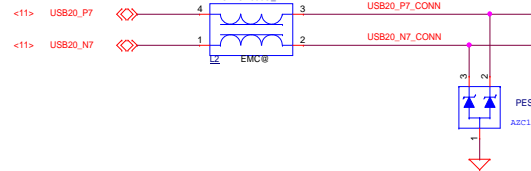
SA0000AQ200 :  
S IC NPCT750JAAAX QFN 32P TPM F/W is 7.1.0.0 - ES  
SA0000AQ220 :  
S IC NPCT750JAAAX QFN 32P TPM F/W is 7.2.0.0 - QS



- Pin14&Pin22 (+3VS\_TPM):  
For NPCT650x: connect to same power well with host SPI interface (it should be +3V\_PCH)  
For NPCT750x: connect to S0 power well (+3VS)
- Pin27:  
For NPCT650x: pop R22  
For NPCT750x: de-pop R22
- SLP\_S0# connection:  
For NPCT650x: pop RE104, de-pop RE2  
For NPCT750x: pop RE2, de-pop RE104
- RC180 can be just deleted for both NPCT650x and NPCT750x
- TPM\_PIRQ# is recommended that pull-up to same GPIO power well at host side

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Date: Tuesday, October 17, 2017		Sheet 27 of 61		Document Number LA-E671P	

## M.2 Slot-A Key-A

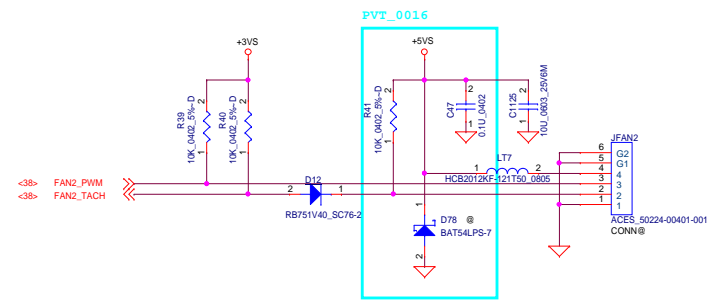


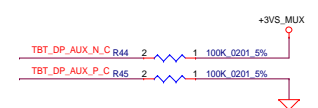
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Issued Date		2015/12/16		Deciphered Date	
		2016/12/13		<b>Compal Electronics, Inc.</b> <b>P28-WLAN / BT</b>	
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				Rev 1.0	
Date:		Tuesday, October 17, 2017		Sheet 28 of 61	



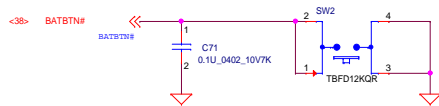
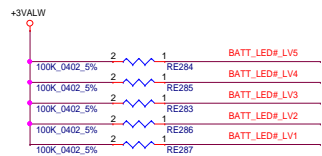
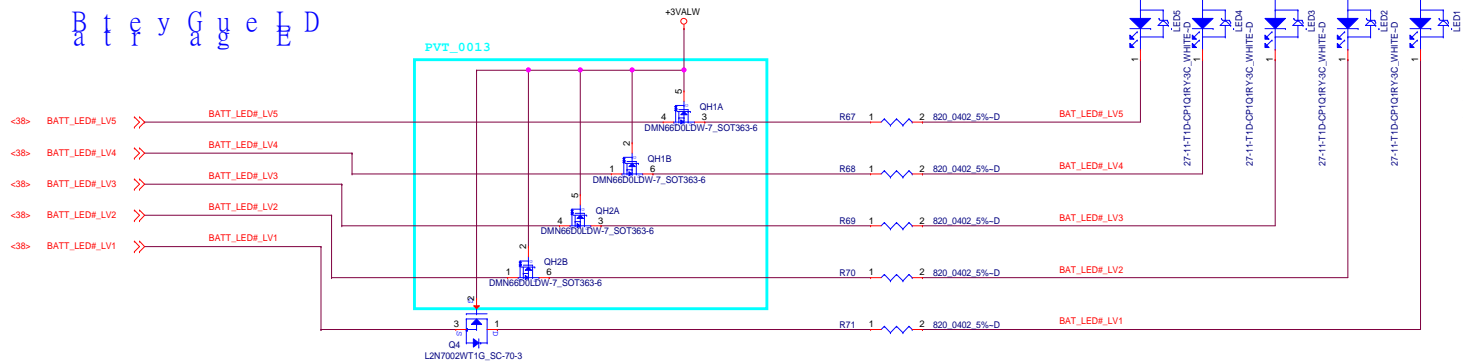
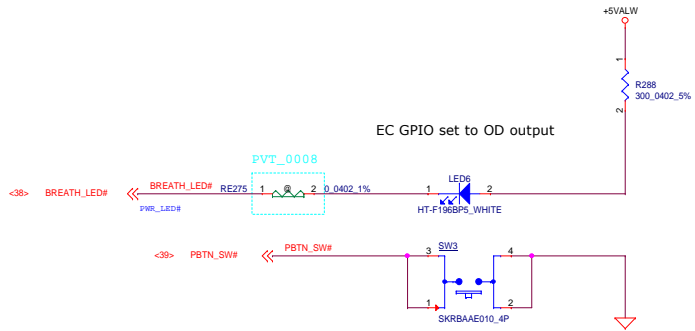
FAN 1



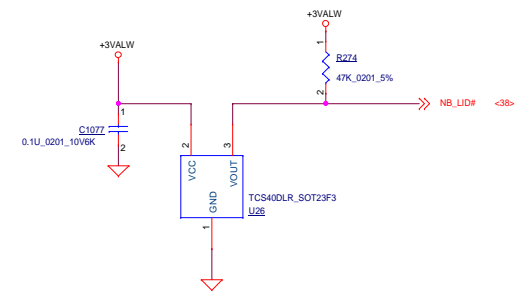


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				Size	Document Number	Rev			
				LA-E671P		1.0			
				Date:	Tuesday, October 17, 2017	Sheet	31	of	61

## Power Button +LED



***NB LID SW***



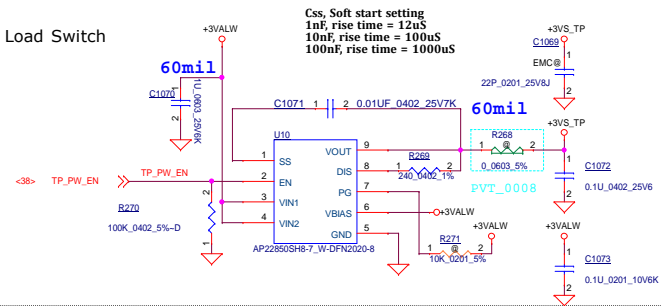
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**Compal Electronics, Inc.**

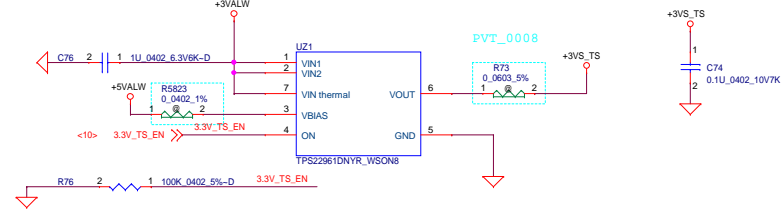
Security Classification		Compal Secret Data		<div style="text-align: right;"> <b>ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE</b> </div>	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	<b>Compal Electronics, Inc.</b>	
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				Size Document Number <b>LA-E671P</b>	
				Date: Tuesday, October 17, 2017 Sheet 32 of 61	



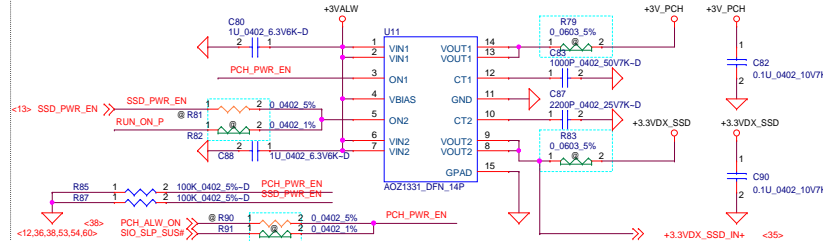
## Touch Pad Load Switch



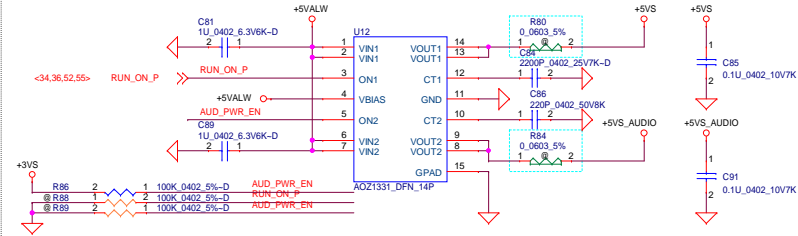
## Touch Screen Load Switch



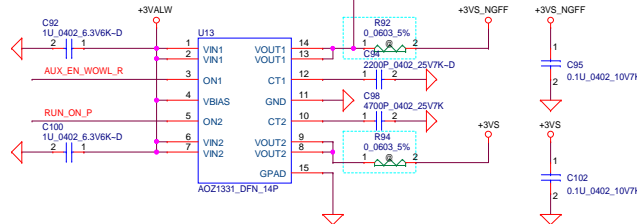
## Deeper Sleep, SSD Load Switch



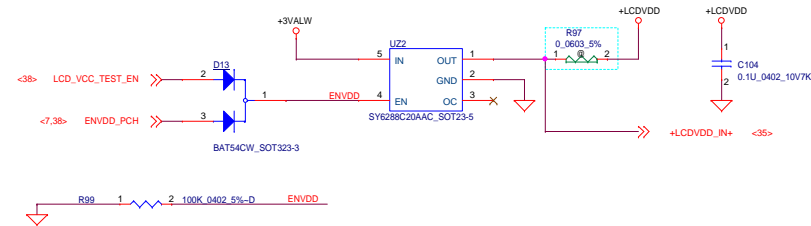
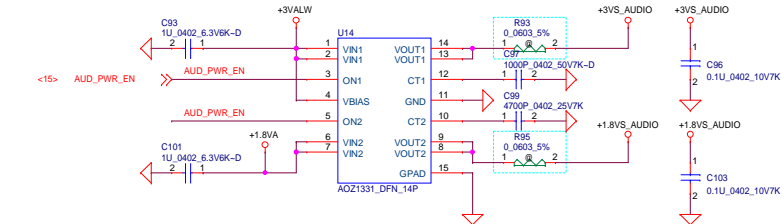
## 5V\_Run, 5V\_Audio Load Switch



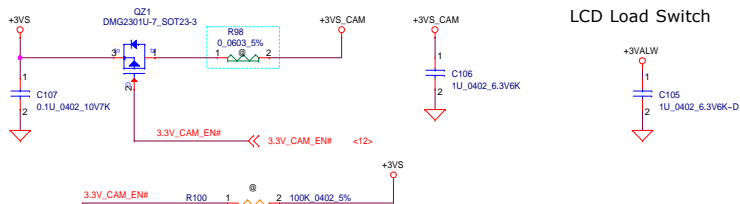
## WiFi, 3V\_RUN Load Switch



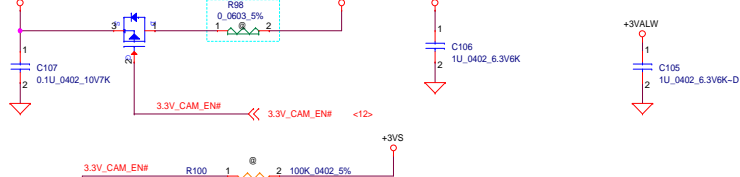
## 3V\_Audio, 1.8V\_Audio Load Switch



## Camera

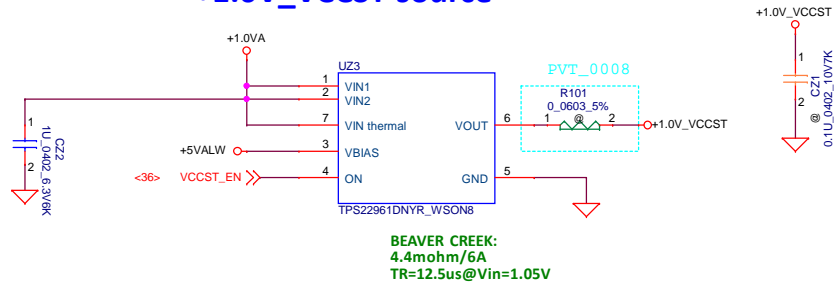


## LCD Load Switch

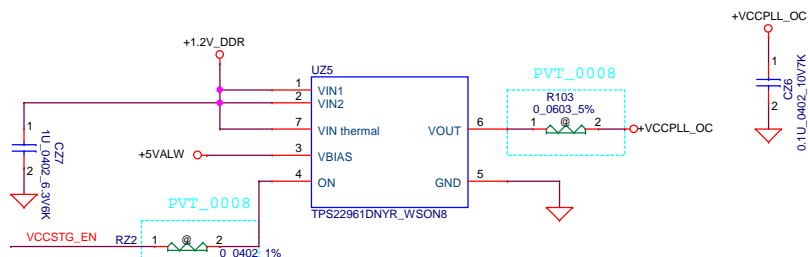


Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		2015/12/16		Compal Electronics, Inc.	
Deciphered Date		2016/12/13		Title	
				P33-DC/DC Interface 1	
				Size	
				LA-E671P	
				Rev	
				1.0	
				Date: Tuesday, October 17, 2017	
				Sheet 33 of 61	

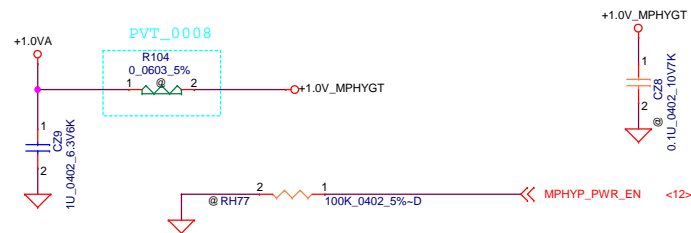
## +1.0V\_VCCST source



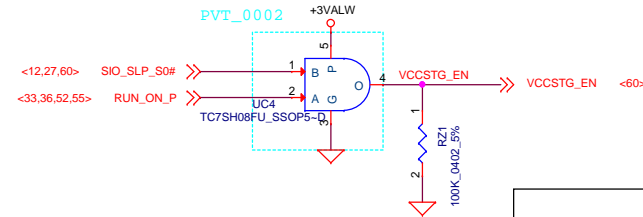
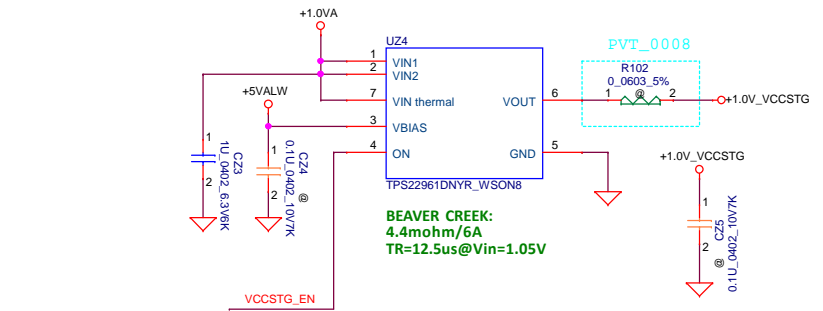
## +VCCPLL\_OC source



## +1.0V\_MPHYGT source



## +1.0V\_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc.			
Issued Date				2015/12/16		Deciphered Date		2016/12/13		Title	
										P34-DC/DC Interface 2	
										Size Document Number	
										LA-E671P	
										Date: Tuesday, October 17, 2017	
										Sheet 34 of 61	
										Rev 1.0	

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# Keyboard Controller board + DMIC

Keyboard Controller board + DMIC

Why? Ambiguity

Place close to JKB1

Use SP010027G00

[illegible]

# RTC Battery With Charge Function

**FD1 FIDUCIAL**  
**FD2 FIDUCIAL**  
**FD3 FIDUCIAL**  
**FD4 FIDUCIAL**

**H22**  
H\_1P8N  
H26  
H\_1P8K2P3N

**Locating holes**

**H13**  
H\_2P0  
**H14**  
H\_2PON  
**H18**  
H\_2PON

**Screw**

**H19**  
H\_1P8  
**H20**  
H\_1P8

**Standoff for WLAN**

**H11**  
H\_2P0  
**H12**  
H\_2P0  
**H21**  
H\_2P0

**Bracket**

**H16**  
H\_2P0  
**H17**  
H\_2P0  
**H23**  
H\_2P0

**Bracket**

**H1**  
H\_3P3  
**H2**  
H\_3P3

**Standoff for eDP**

**H25**  
H\_1P2X1P7N

**H3**  
H\_3P3  
**H4**  
H\_3P3  
**H5**  
H\_3P3  
**H6**  
H\_3P3

**Standoff for CPU Cooler**

**H7**  
H\_3P3

**Standoff for SSD**

**H8**  
H\_2P6  
**H9**  
H\_2P6

**Standoff for FAN**

**H24**  
CLIP\_C6-PM

**For PCB shielding**

**For AR shielding**

**For PCB shielding**

**Classification**  
Confidential

**Deciphered Date**  
2016/12/13

**Classification**  
Confidential

**Deciphered Date**  
2016/12/13

**Title**  
P35-ScrewHole/KB/RTC/IR T/PWRM

**Size**  
Document Number

**Date**  
Tuesday, October 17, 2017

**Sheet**  
35 of 61

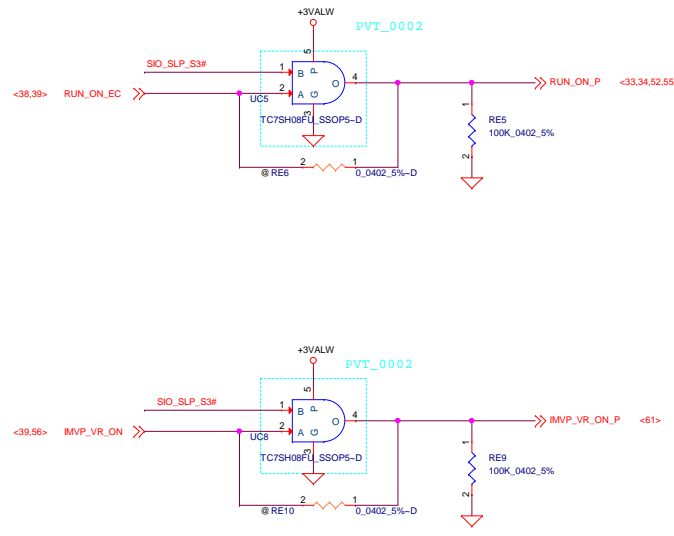
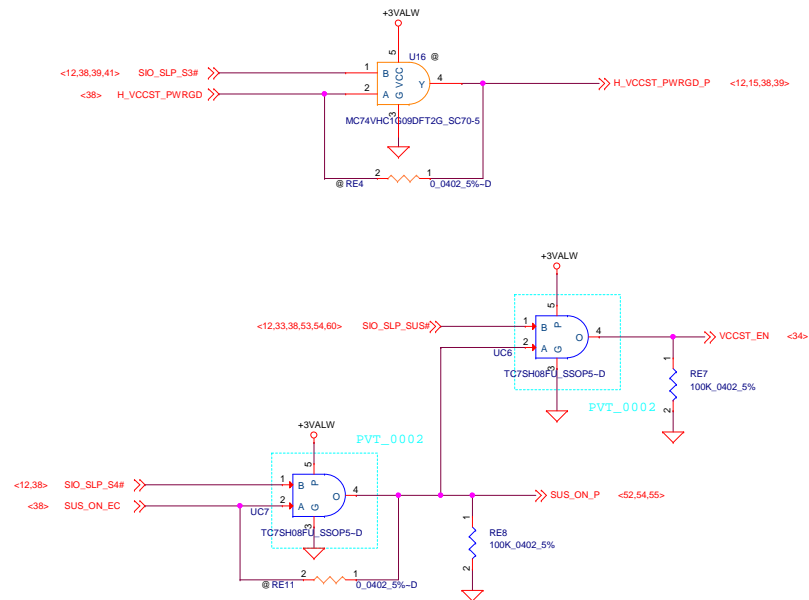
**Rev**  
1.0

**Compal Electronics, Inc.**

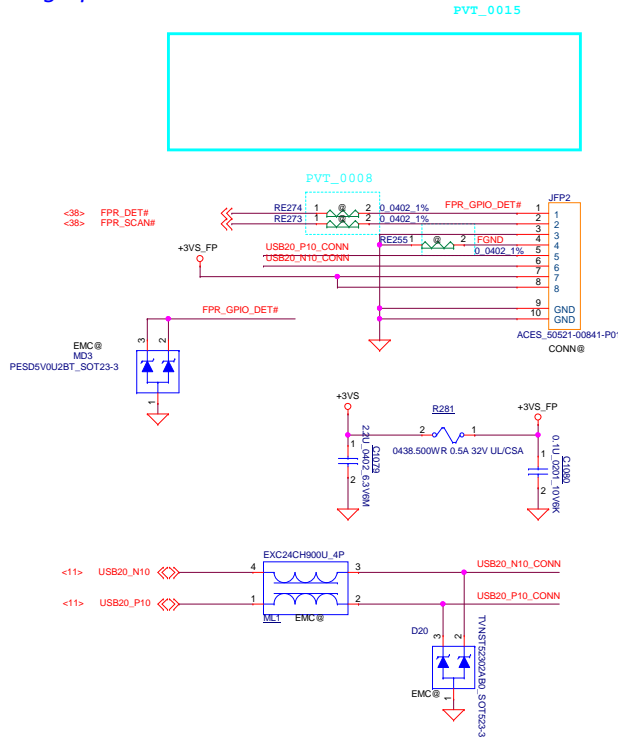
**P35-SCREWH/KB/RTC/IR T/PWRM**

Document Number <b>LA-E671P</b>	Rev 1.0
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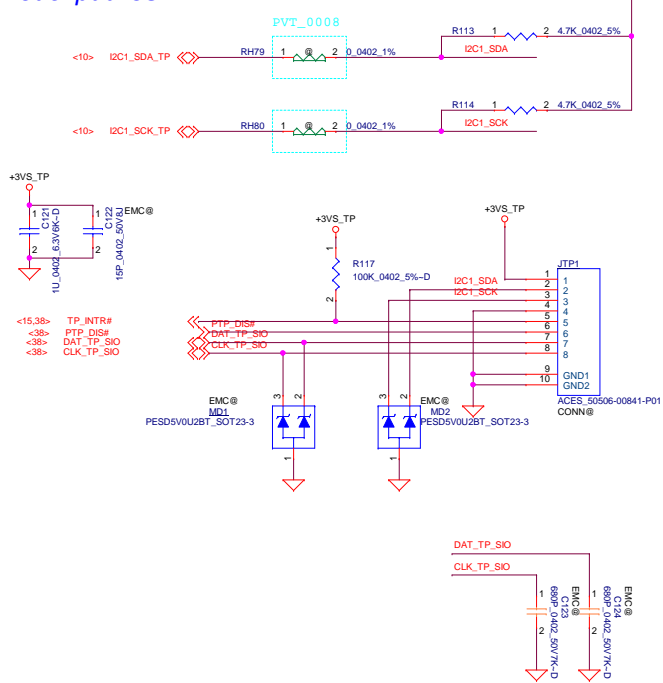
Date:	Tuesday, October 17, 2017	Sheet	35	of	61
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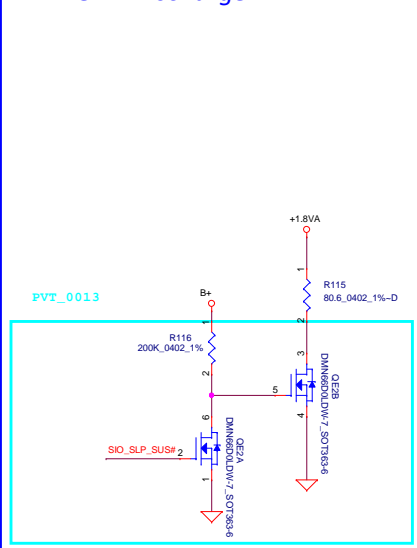
## Fingerprint CONN



## Touchpad CONN

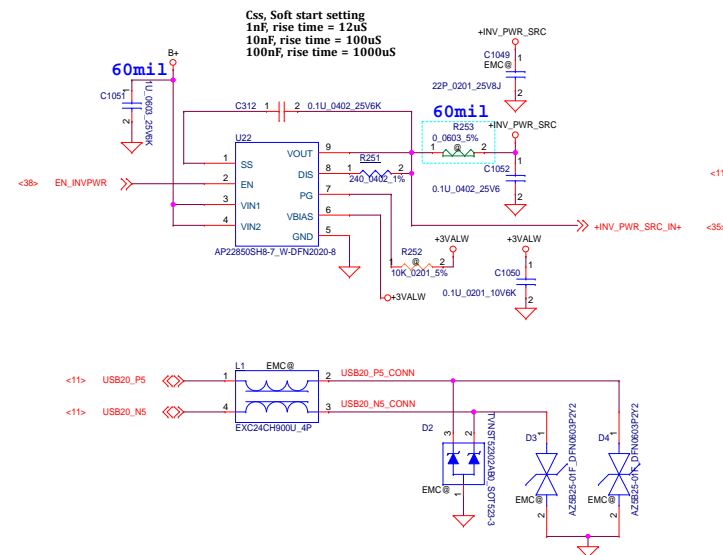


## +1.8VA Discharge

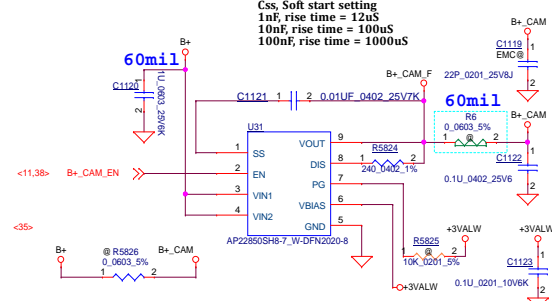


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DELL CONFIDENTIAL/PROPRIETARY		Compal Electronics, Inc.	
Title		P36-TP/FP/PWGRGD	
Size	Document Number	Rev 1.0	
Date: Tuesday, October 17, 2017		Sheet	36 of 61

Css, Soft start setting  
1nF, rise time = 12uS  
10nF, rise time = 100uS  
100nF, rise time = 1000uS



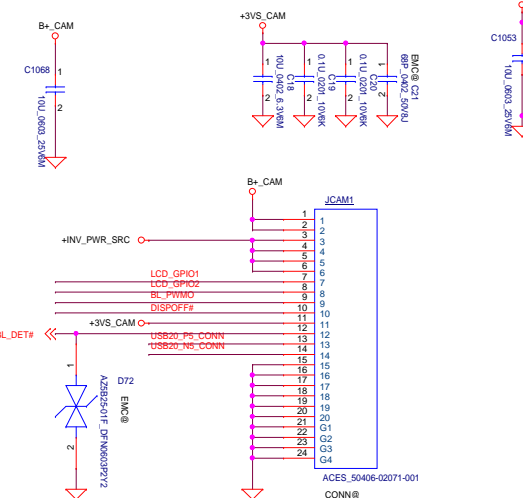
Css, Soft start setting  
1nF, rise time = 12uS  
10nF, rise time = 100uS  
100nF, rise time = 1000uS



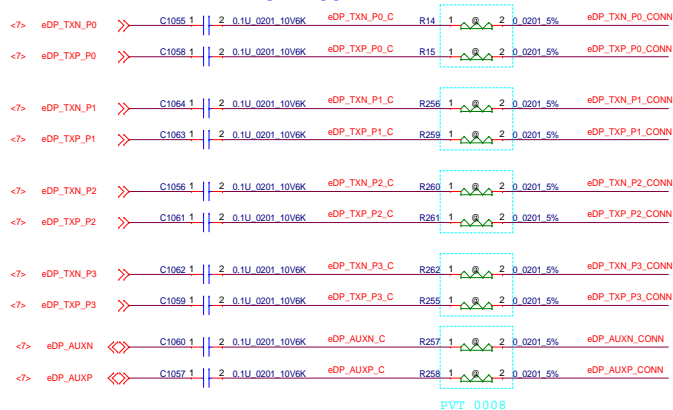
CAM & IR CAM

LCD BL Power

CAM & IR CAM

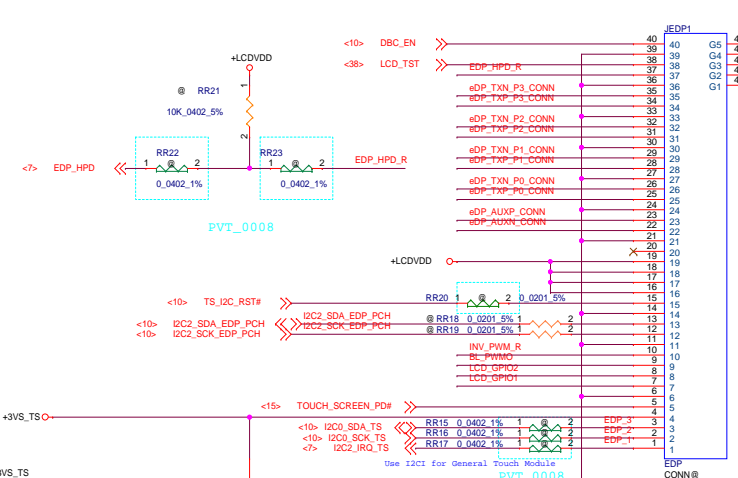
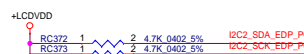
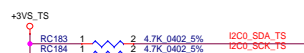
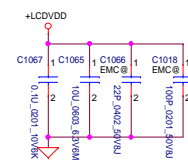
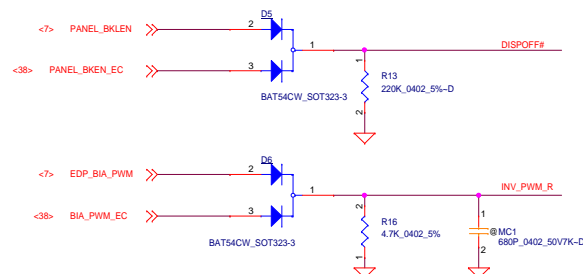


## eDP Conn



PVT\_0008

## BackLight PWM Control



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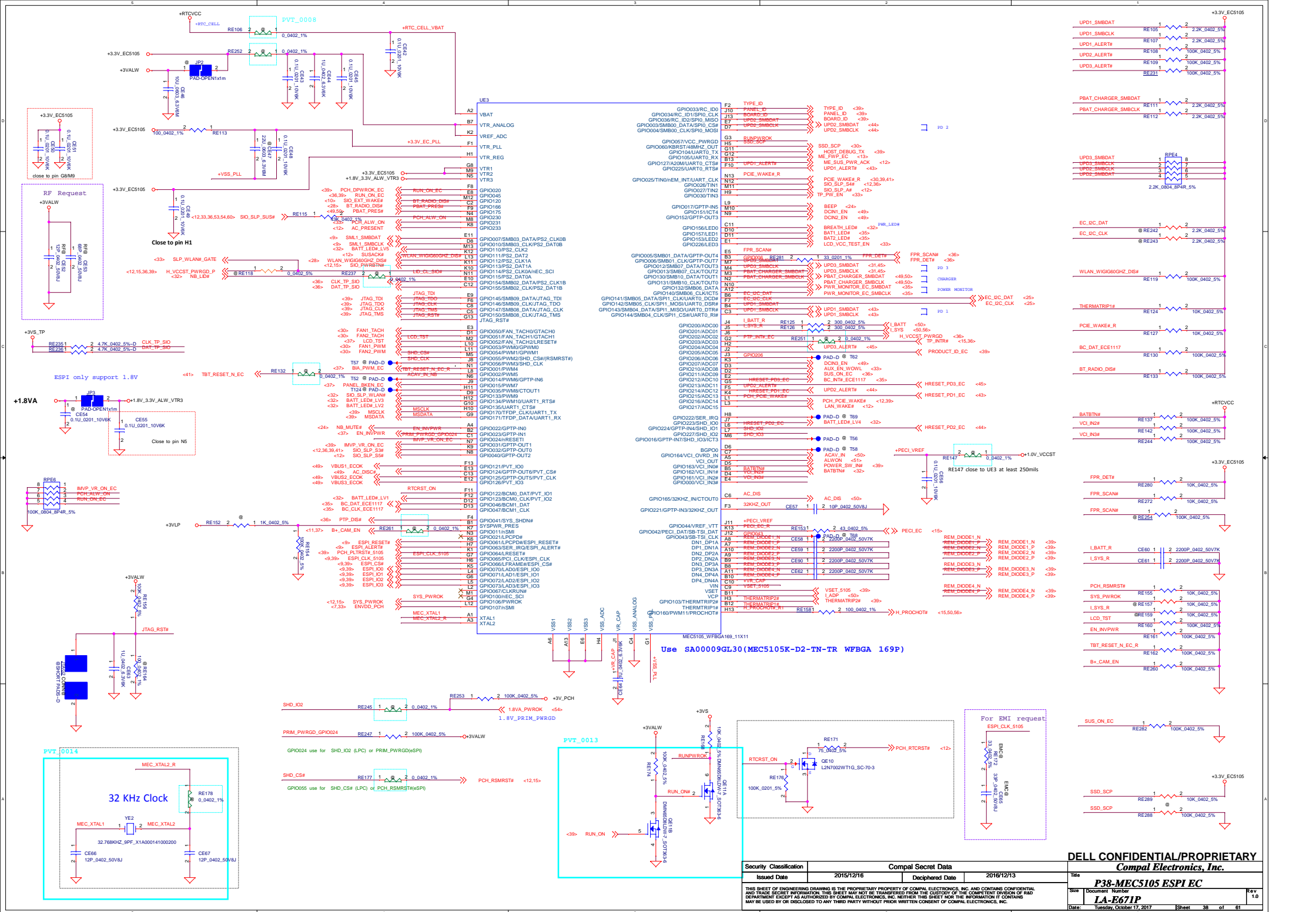
Compal Electronics, Inc.

P37-eDP+TS & CAM+BL CONN

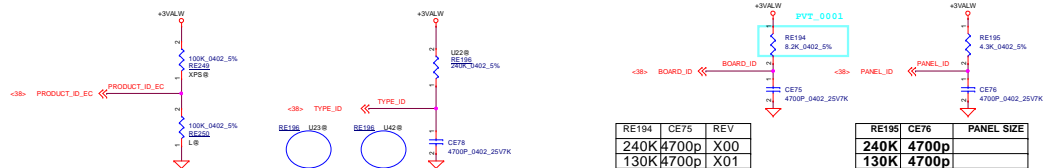
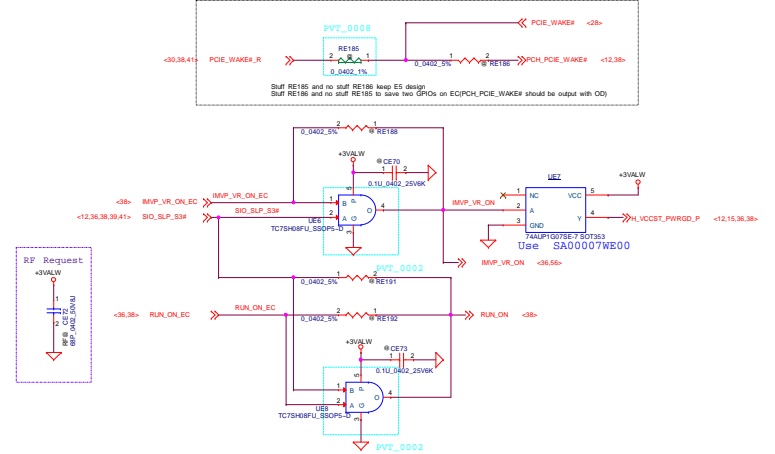
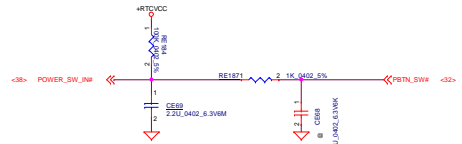
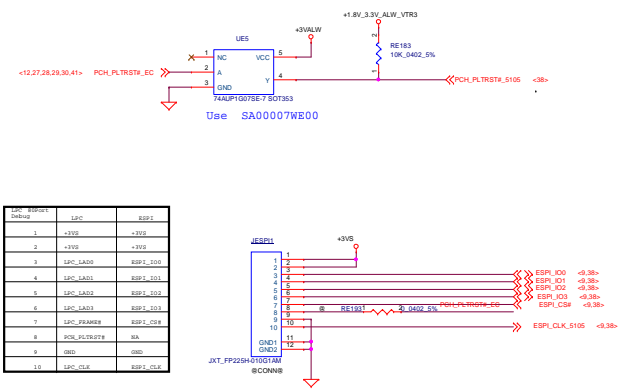
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QFN Pinout	QFN	QFN
1	VDD	VDD
2	VDD	VDD
3	VDD	VDD
4	VDD	VDD
5	VDD	VDD
6	VDD	VDD
7	VDD	VDD
8	VDD	VDD
9	VDD	VDD
10	VDD	VDD

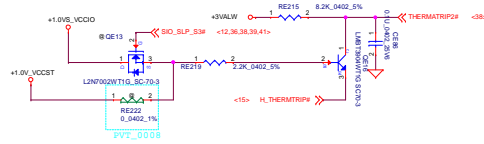
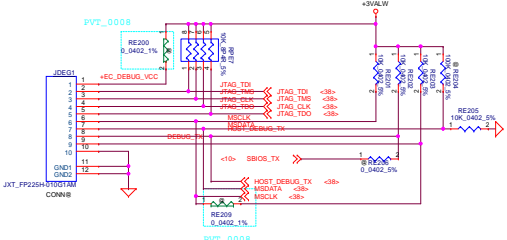


RE249	RE250	REV
@	@	Italia XPS
@	@	Italia-L

RE196	CE78	REV
240K	4700p	U2+2
130K	4700p	U2+3e
62K	4700p	U4+2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

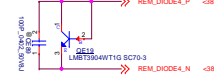
RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

RE195	CE76	PANEL SIZE
240K	4700p	
130K	4700p	
33K	4700p	
4.3K	4700p	Italia 13

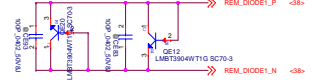


5105 Channel	Location
DP1/DN1	OTP (QE12)
SEN4	DN1a/DP1a Charger (QE20)
SEN1	DP2/DN2 DDR (QE14)
SEN5	DN2a/DP2a SKIN (QE21)
SEN6	DP3/DN3 SKIN (QE22)
SEN2	DN3a/DP3a SSD (QE15)
SEN3	DP4/DN4 WLAN (QE19)
	DN4a/DP4a

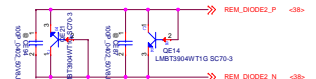
DP4/DN4 for WLAN on QE19, place QE19 close to WLAN & QE19 close to CE89.



DP1/DN1 for CPU Place CE83 close to the QE12 as possible

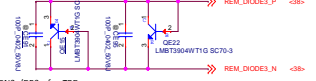


DP2/DN2 for DDR on QE14, place QE14 close to DDR and CE87 close to QE14



DN2a/DP2a for SKIN. Place CE84 close to QE21

DP3/DN3 for SSD Place CE91 close to the QE15 as possible



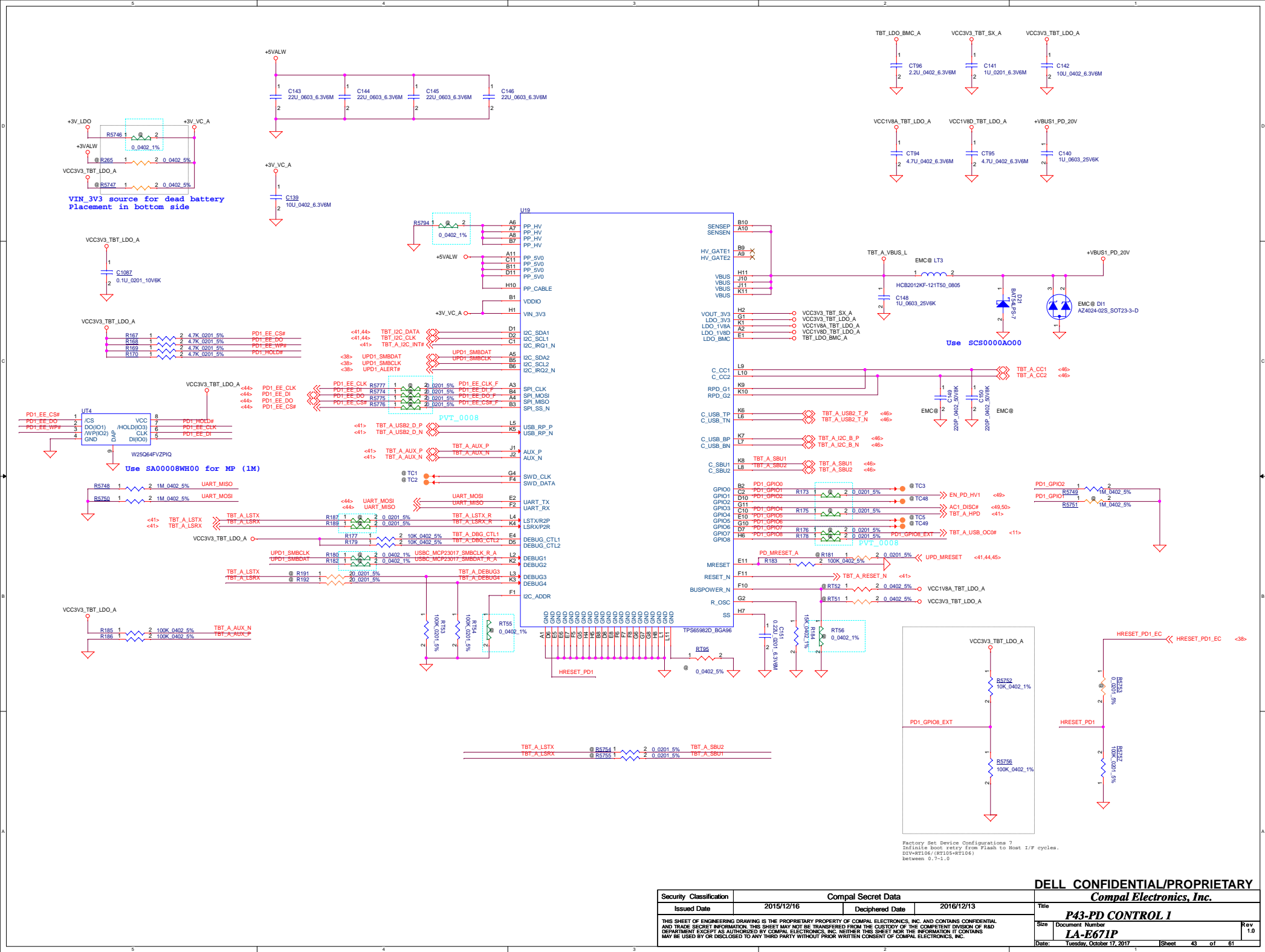
DN3a/DP3a for TSD. Place CE95 close to QE22





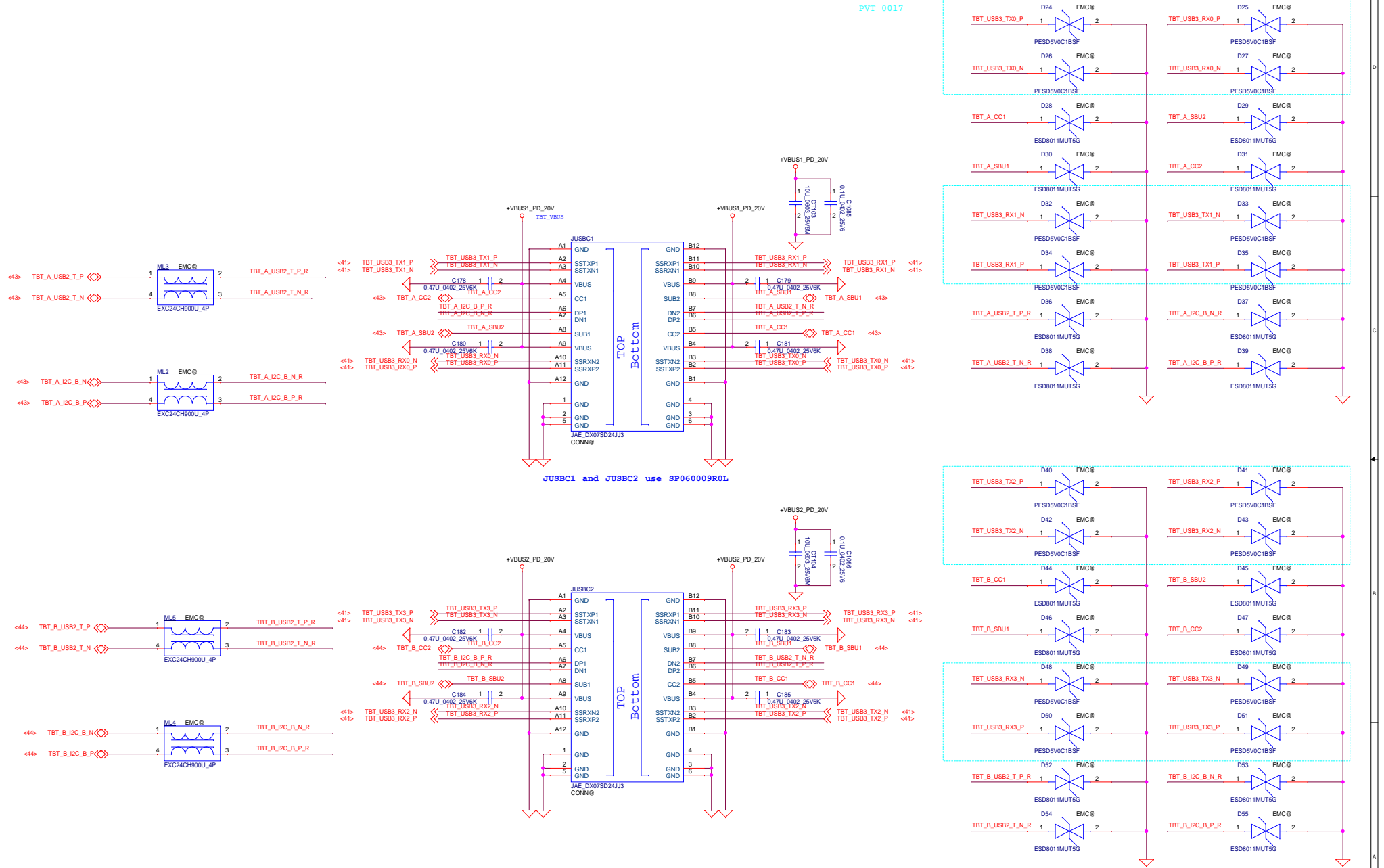


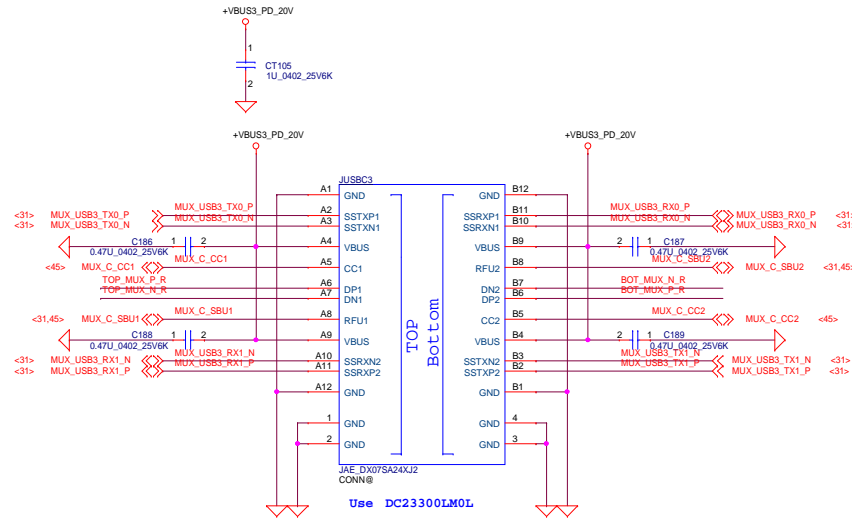
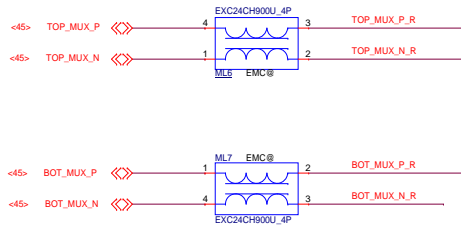




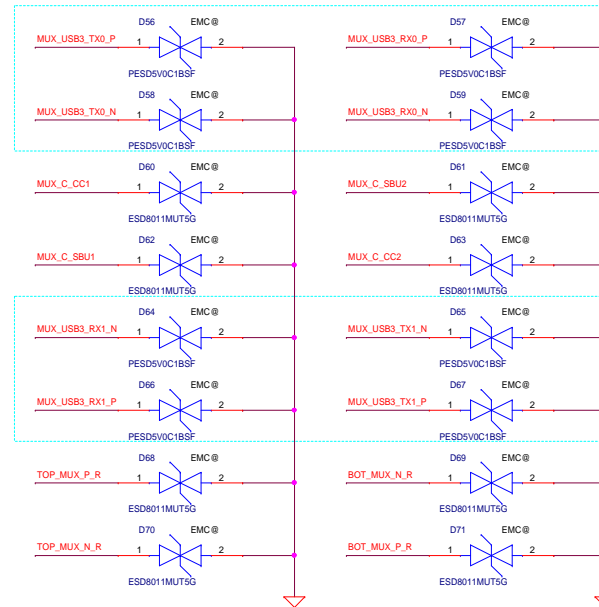


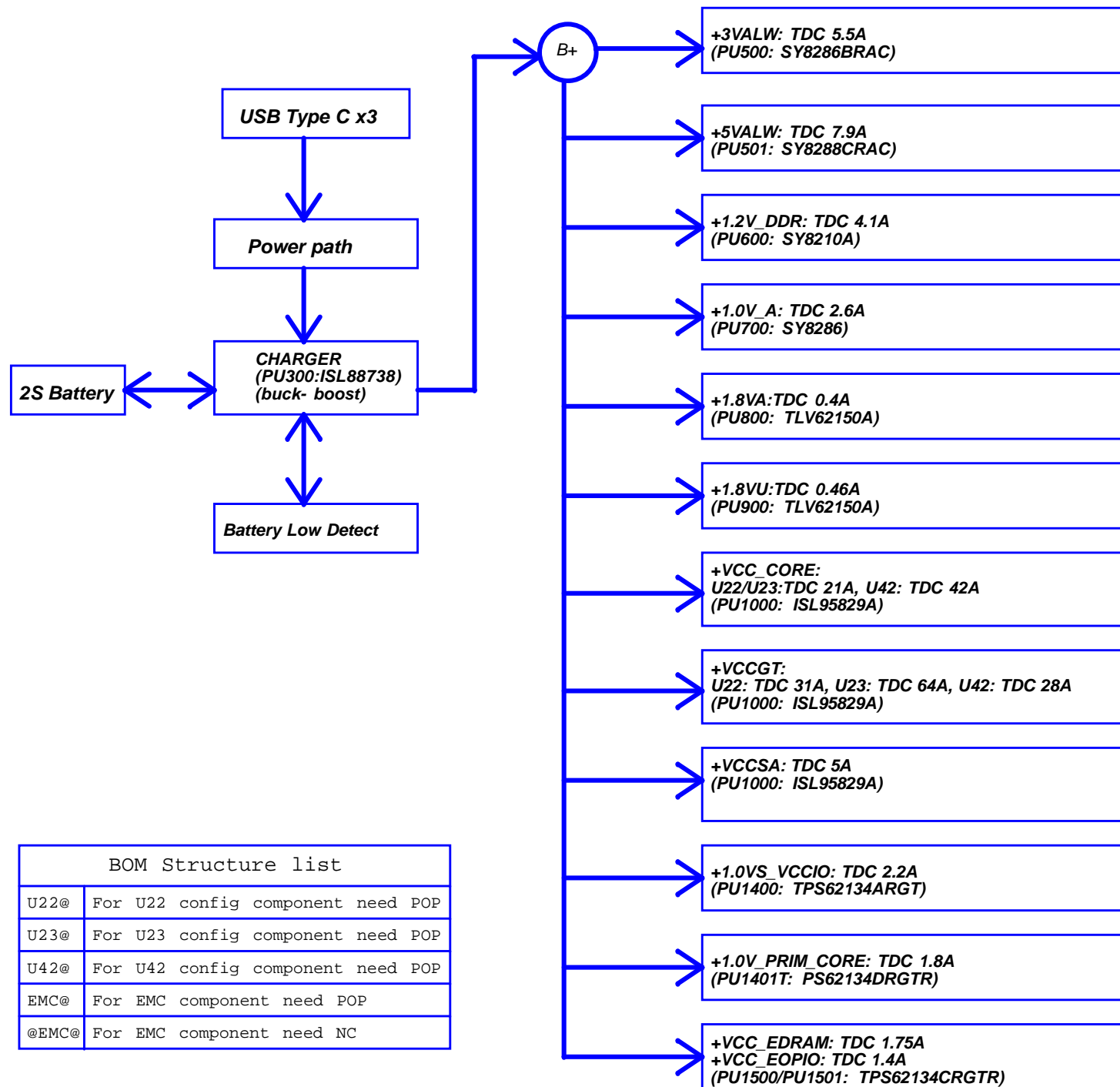




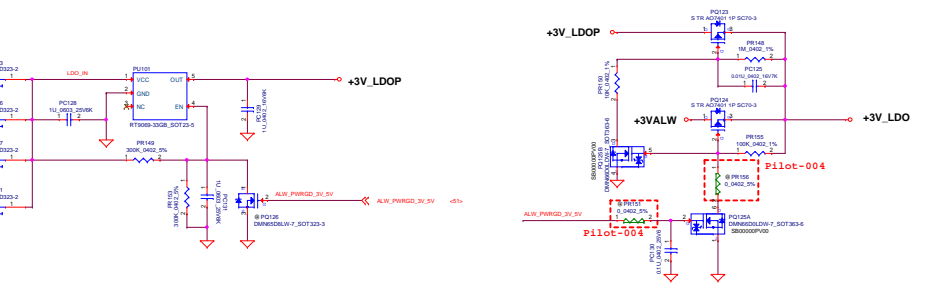
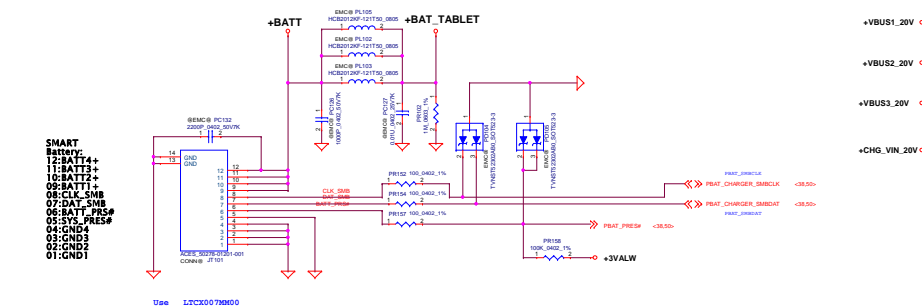


PVT\_0017

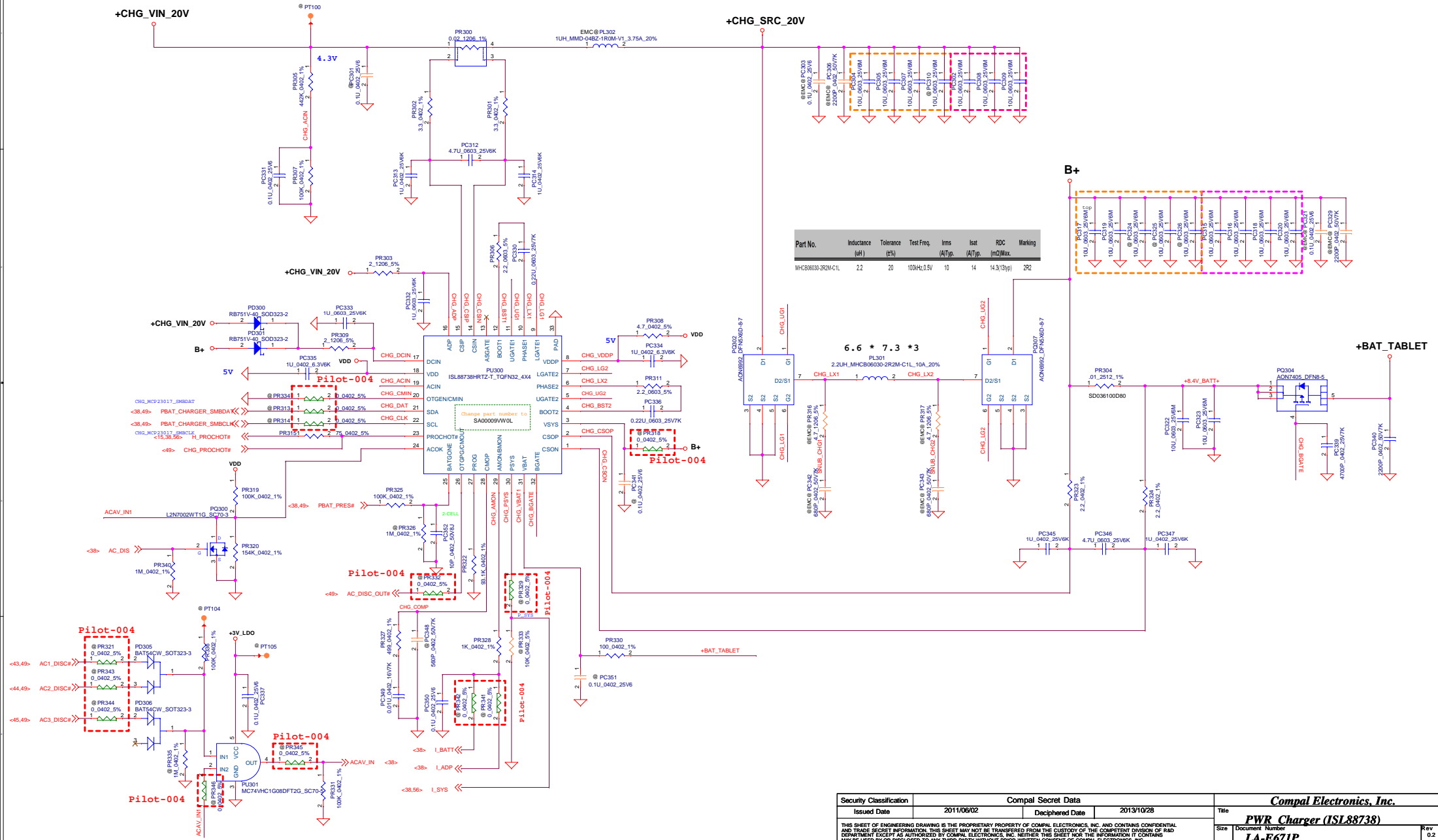


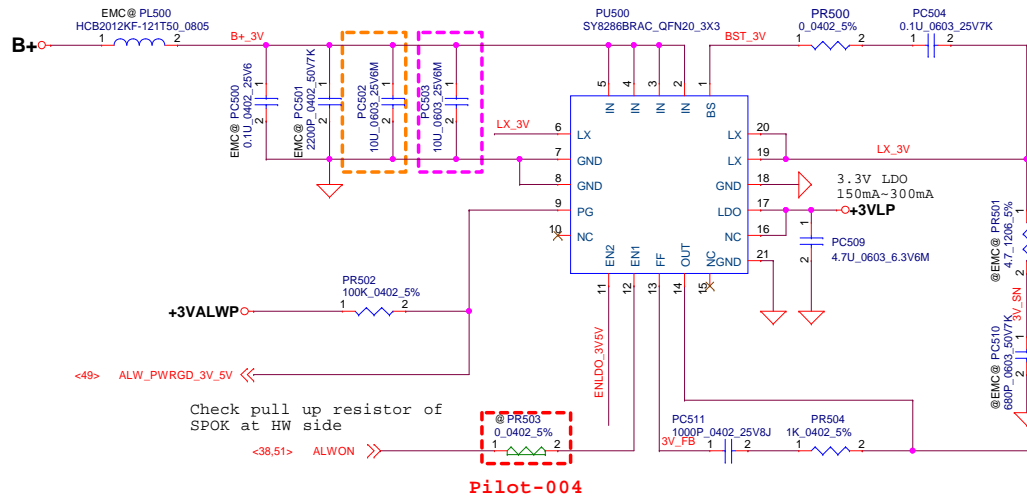




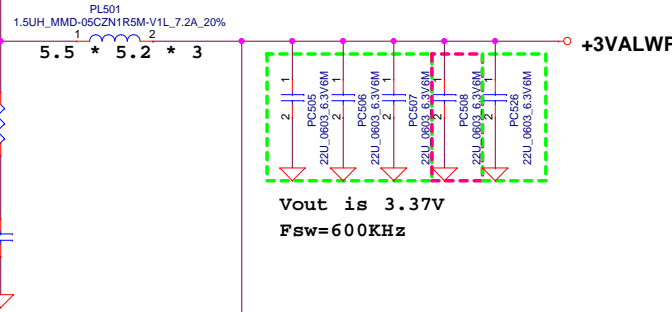


Title		<b>DCIN/Power Path</b>
Size	Document Number	
	<b>LA-E671P</b>	



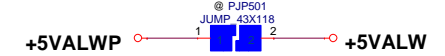
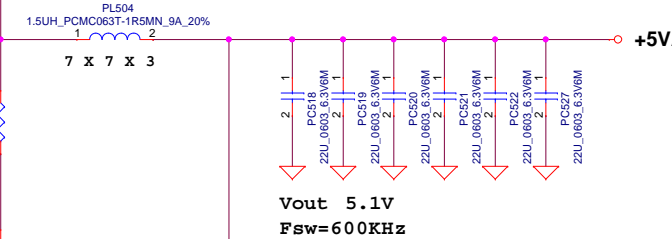
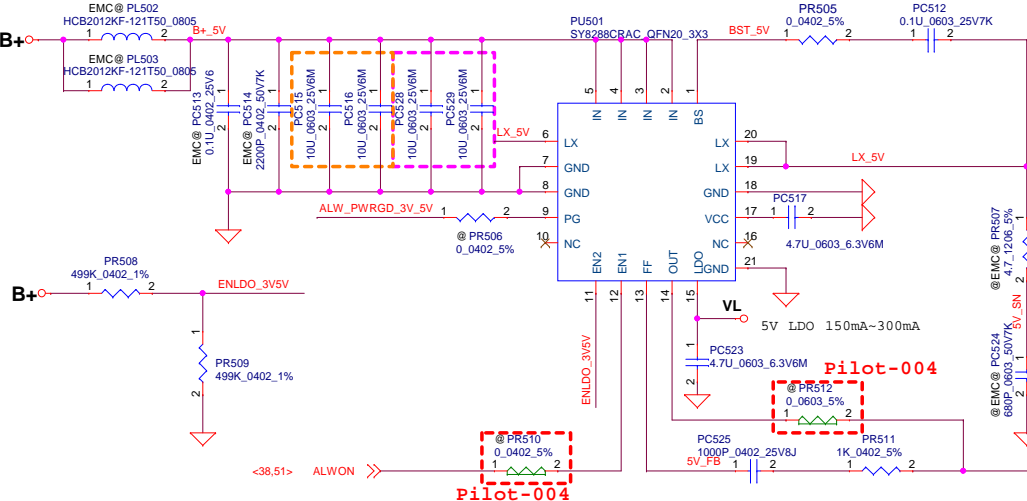


P/N	L*W(mm*mm)	H(mm)	LX(μH)	RDC(mΩ)	I <sub>ds</sub> (A)	I <sub>sat</sub> (A)
MMD-05CZ-1R5M-V1L	5.49*5.18	3	1.5	19.7	20.7	7.2



3VALWP  
TDC 5.2A  
Peak Current 7.5A  
OCP Current 8.0A (fix)

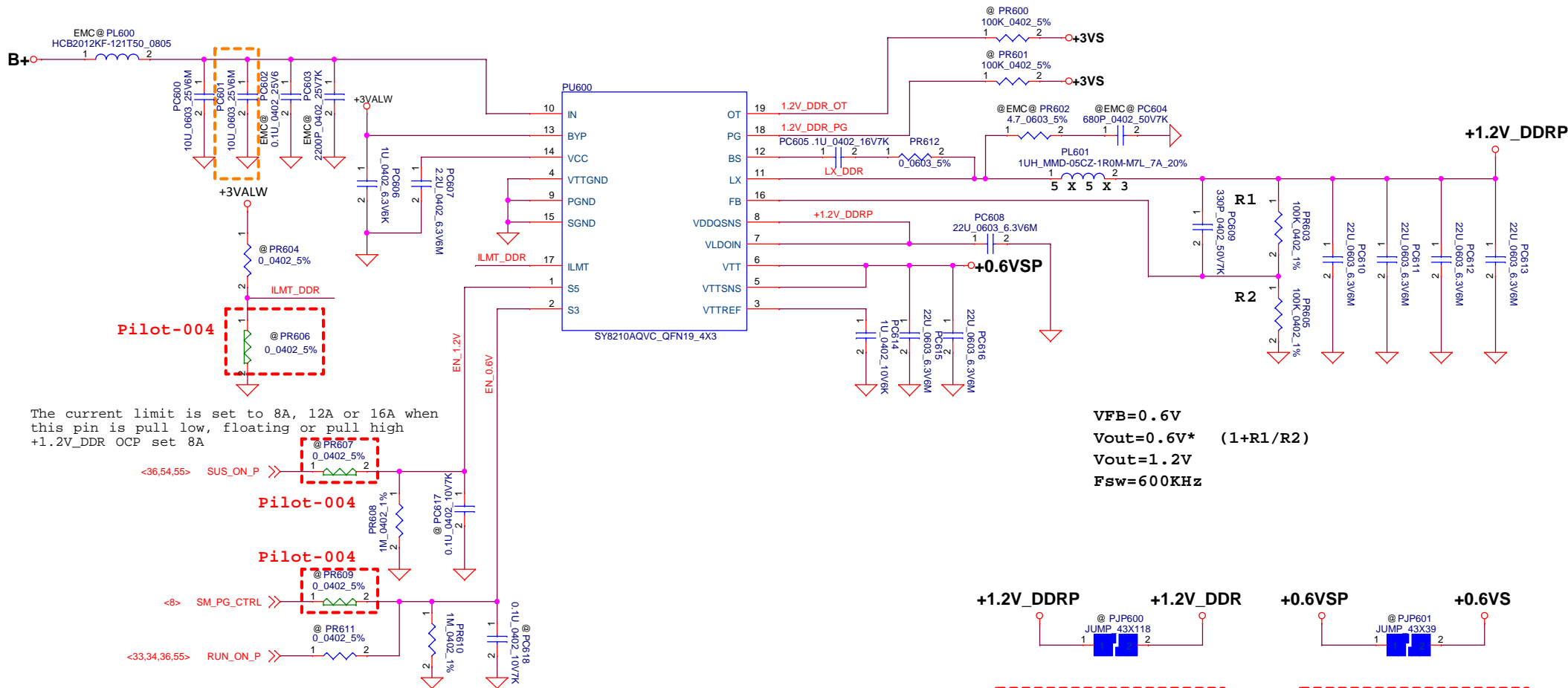
Non AR  
3VALWP  
TDC 5.5A  
Peak Current 7.5A  
OCP Current 8.0A (fix)



5VALWP  
TDC 7.9A  
Peak Current 11.0A  
OCP Current 13.0A

3V/5V controller(35.1), Support component(35.2)

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$V_{FB} = 0.6V$   
 $V_{out} = 0.6V * (1 + R1/R2)$   
 $V_{out} = 1.2V$   
 $F_{sw} = 600KHz$

**+1.2V\_DDR**  
 TDC 4.1A  
 Peak Current 5.8A  
 OCP Current 8A

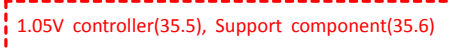
0.6Volt +/- 5%  
 TDC 0.4A  
 Peak Current 0.6A  
 OCP Current 2A (fix)

DDR controller(35.3), Support component(35.4)

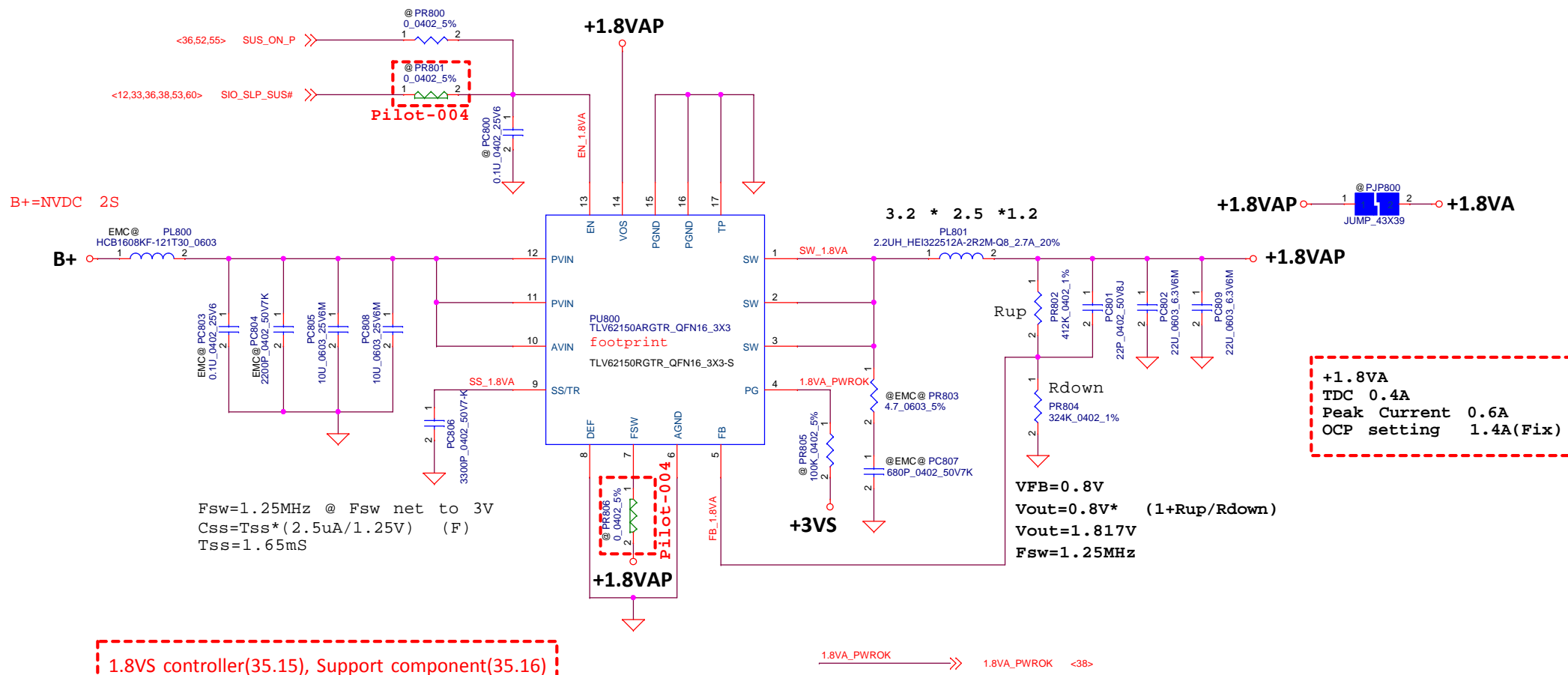
Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

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				Size	Document Number
				<b>LA-E671P</b>	
Date: Tuesday, October 17, 2017				Sheet	52 of 61

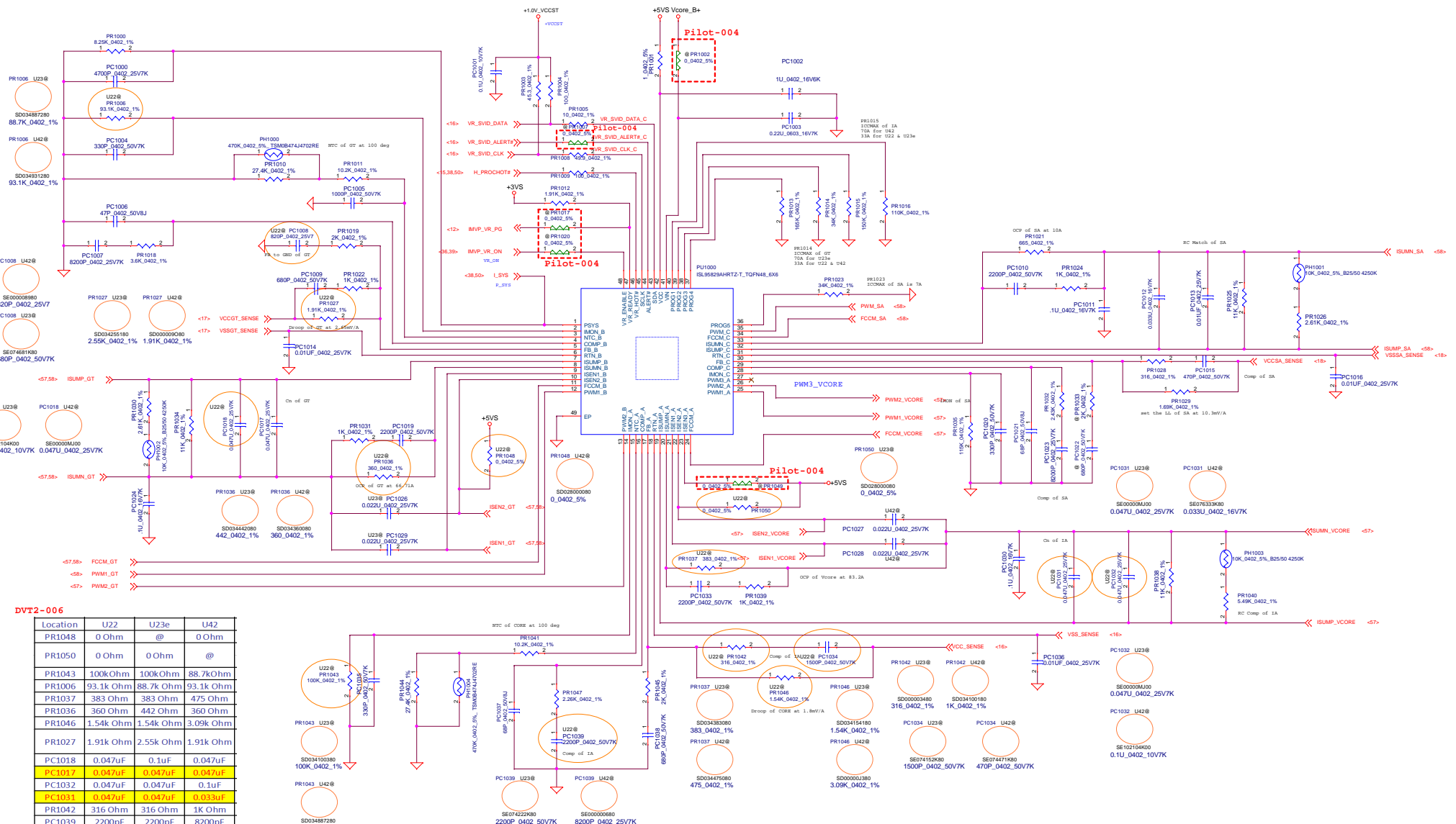


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					<b>LA-E67IP</b>
				Date:	Tuesday, October 17, 2017
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				Size	Document Number	Rev
				LA-E671P		0.4
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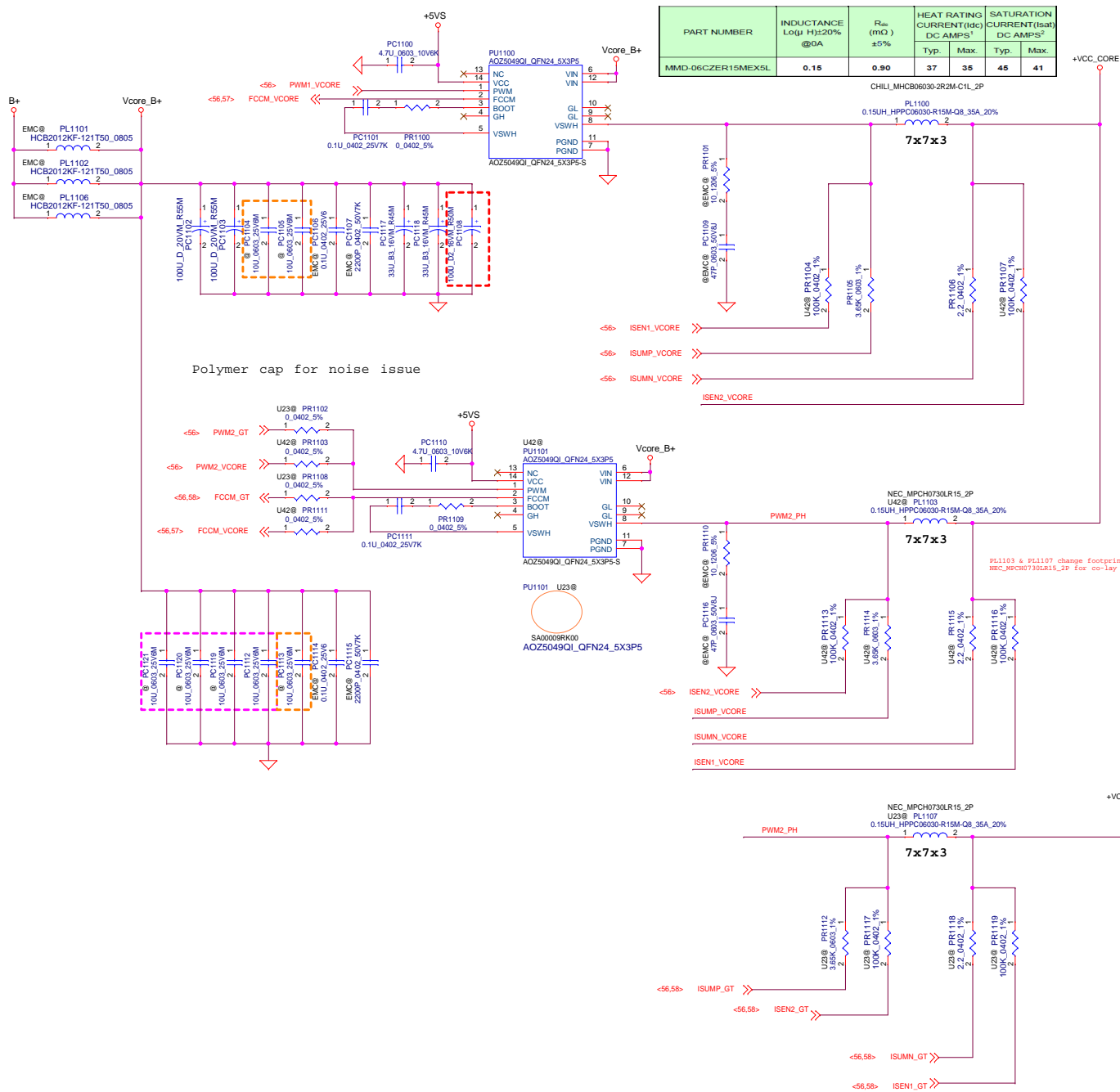
DVT2-006

Location	U22	U23e	U42
PR1048	0 Ohm	@	0 Ohm
PR1050	0 Ohm	0 Ohm	@
PR1043	100k Ohm	100k Ohm	88.7k Ohm
PR1006	93.1k Ohm	88.7k Ohm	93.1k Ohm
PR1037	383 Ohm	383 Ohm	475 Ohm
PR1036	360 Ohm	442 Ohm	360 Ohm
PR1046	1.54k Ohm	1.54k Ohm	3.09k Ohm
PR1027	1.91k Ohm	2.55k Ohm	1.91k Ohm
PC1018	0.047uF	0.1uF	0.047uF
PC1017	0.047uF	0.047uF	0.047uF
PC1032	0.047uF	0.047uF	0.1uF
PC1031	0.047uF	0.047uF	0.033uF
PR1042	316 Ohm	316 Ohm	1K Ohm
PC1039	2200pF	2200pF	8200pF
PR1040	5.49 KOhm	5.49 KOhm	5.49 KOhm
PC1034	1500pF	1500pF	470pF
PC1008	820pF	680pF	820pF

CPU Vcore controller(36.1), Drivers(36.2), Support component(36.3)  
Acoustic Noise B+ Bulk CAP(37.2)

Security Classification	2014/10/17	Compal Secret Data	2014/12/05
Issued Date		Deciphered Date	
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Title		Compal Electronics, Inc.	
Size		Vcore ISL95829	
Document Number		LA-E671P	
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PART NUMBER	INDUCTANCE Lo(μH)±20% @0A	Rdc (mΩ) ±5%	HEAT RATING CURRENT(1dc) DC AMPS <sup>1</sup>		SATURATION CURRENT(Isat) DC AMPS <sup>2</sup>	
			Typ.	Max.	Typ.	Max.
MMD-06CZER15MEXSL	0.15	0.90	37	35	45	41

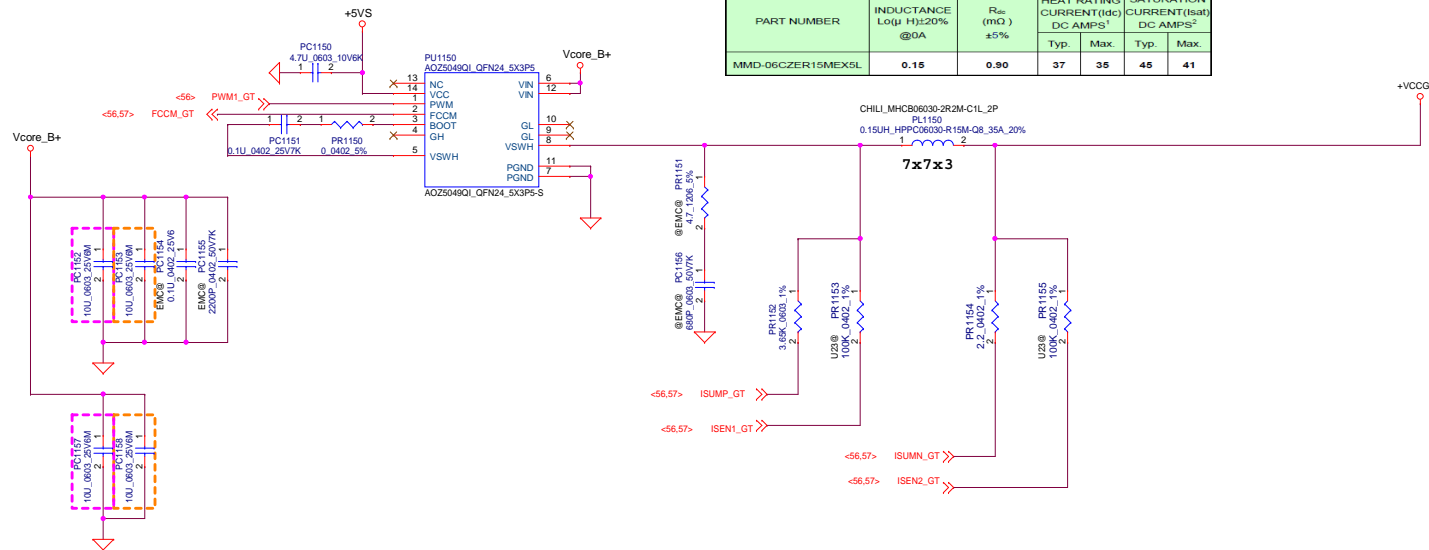
	KBL-RU42 rev.1.6 PAG	KBL-U22 (GT1/GT2) rev.1.5 EDS rev.1.6 PAG	KBL-U23e rev.1.5 EDS rev.1.6 PAG
IA+ring ICCM64	29/32	29	
IA+ring TDC	42	21	
IA+ring di[A]	55	25	
IA+ring DC/A2.4	2.4	2.4	
GT ICCMAX	28	31	64 for merged VR
GT TDC[A]	18	18	38 for merged VR
GT di[A]	20	28	46
GT DC/AC L	3.1	3.1	2
SA ICCMAX	5	4.5	5.1
SA DC/AC L	10.3	10.3	10.3
PL2 extreme	51	29/32	43
PL4 extreme	71	51	66

CPU\_Vcore controller(36.1), Drivers(36.2), Support component(36.3)  
CPU\_Core output CAP(36.4), Acoustic Noise B+ Bulk CAP(37.2)

VCC\_GT (U-line 22)  
TDC 18A  
Peak Current 31A  
OCP current 37A

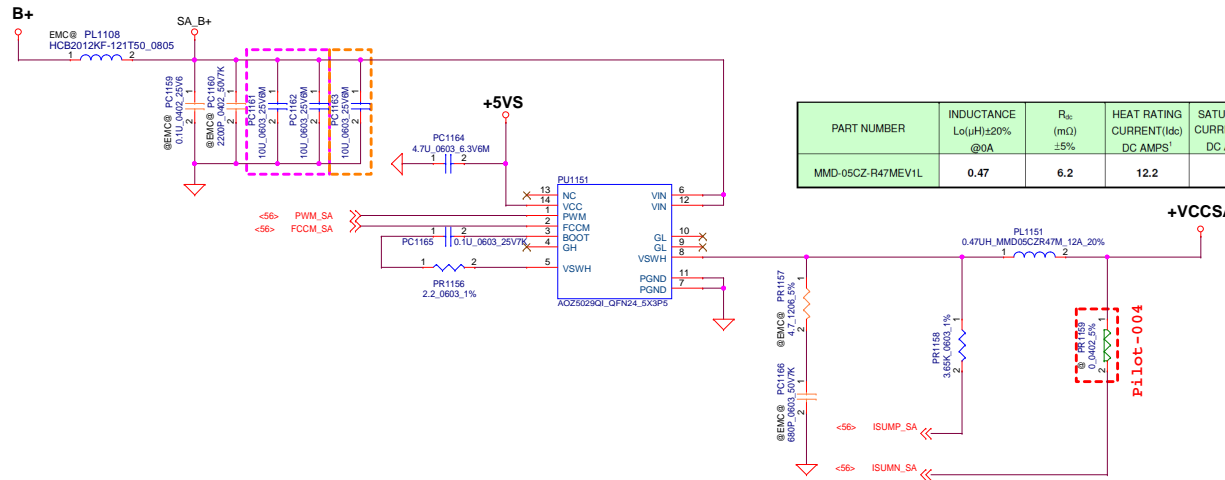
VCC\_GT Merged(GT+GTx)(U-line 23e)  
TDC 35A  
Peak Current 64A  
OCP current 74A

PART NUMBER	INDUCTANCE Lo( $\mu$ H) $\pm$ 20% @0A	R <sub>dc</sub> (m $\Omega$ ) $\pm$ 5%	HEAT RATING CURRENT(I <sub>dc</sub> ) DC AMPS <sup>2</sup>		SATURATION CURRENT(I <sub>sat</sub> ) DC AMPS <sup>2</sup>	
			Typ.	Max.	Typ.	Max.
MMD-06CZER15MEX5L	0.15	0.90	37	35	45	41

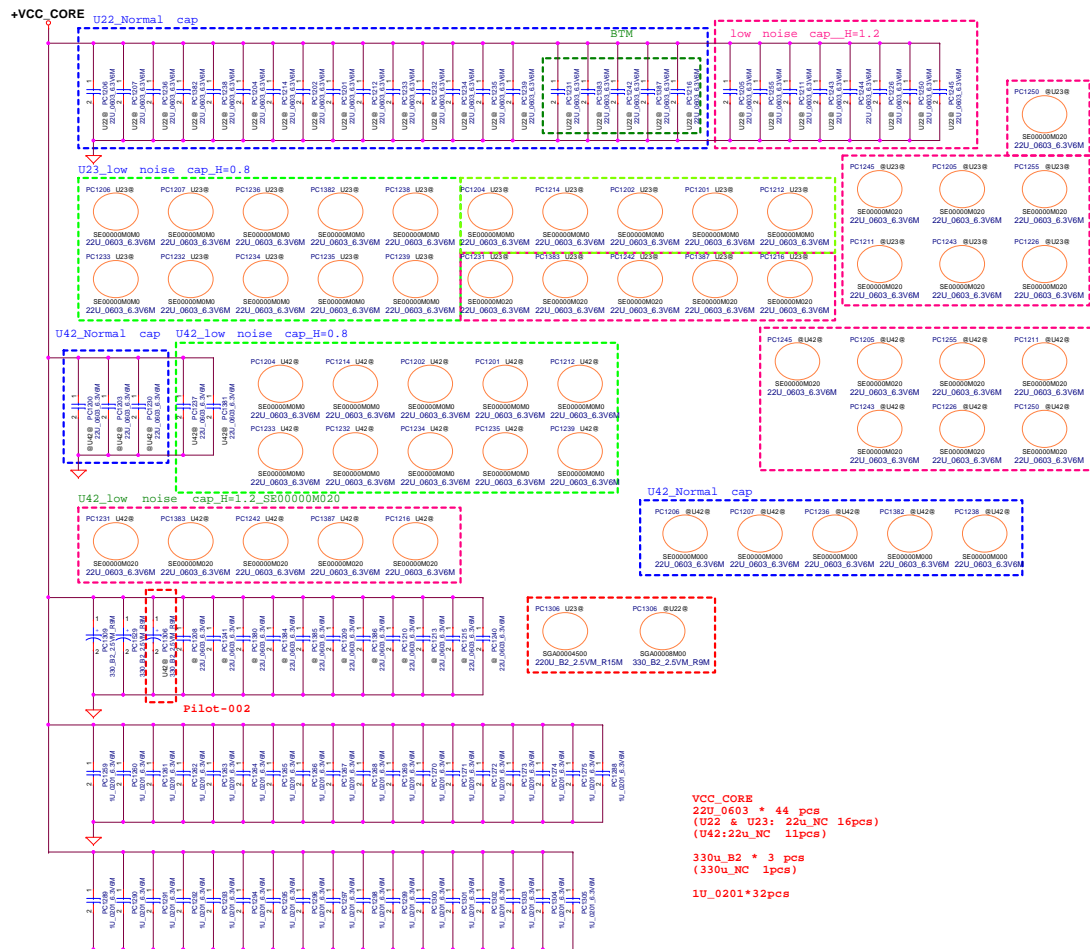


VCC\_SA  
TDC 5A  
Peak Current 5.1A  
OCP current 7A

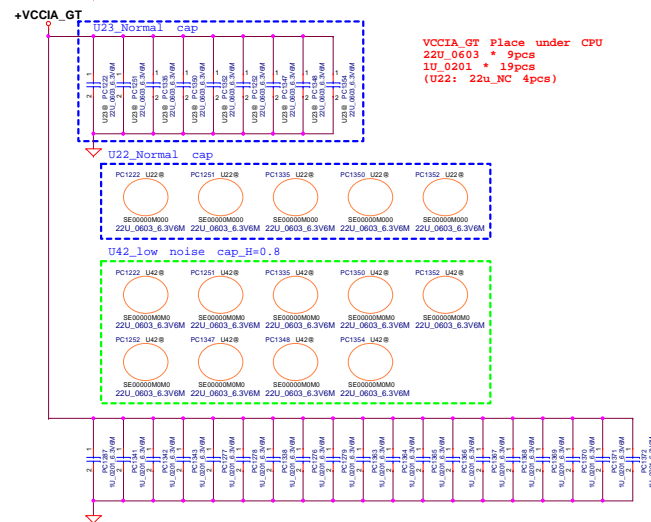
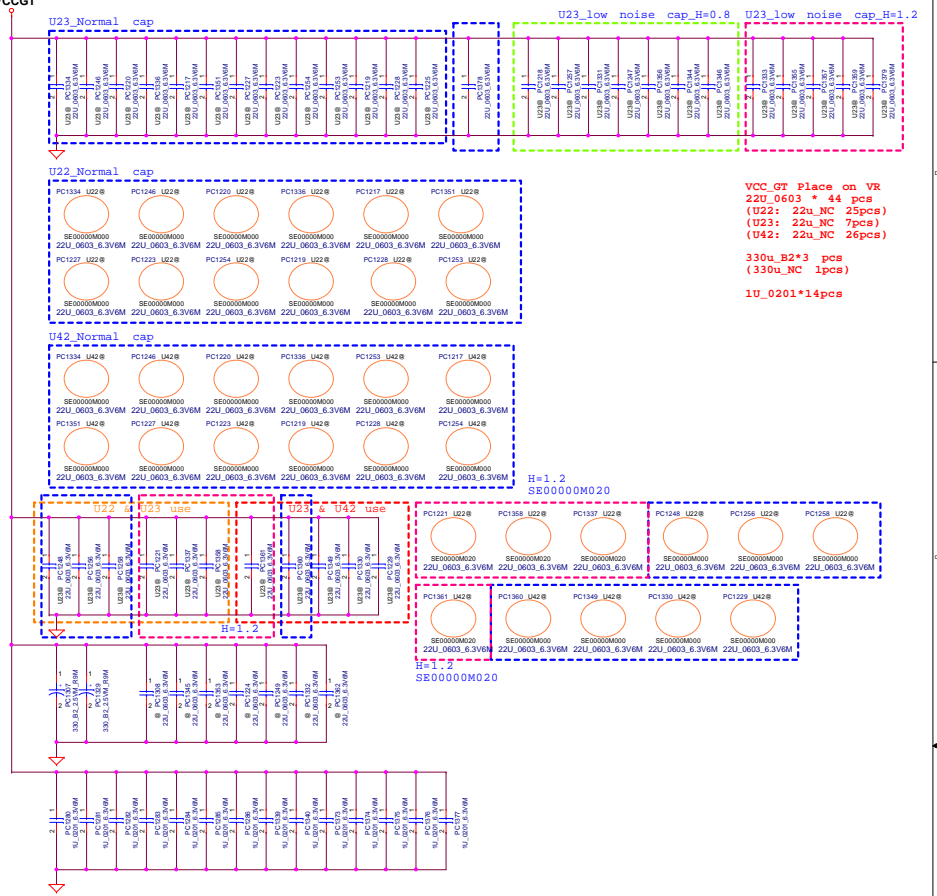
PART NUMBER	INDUCTANCE Lo( $\mu$ H) $\pm$ 20% @0A	R <sub>dc</sub> (m $\Omega$ ) $\pm$ 5%	HEAT RATING CURRENT(I <sub>dc</sub> ) DC AMPS <sup>2</sup>		SATURATION CURRENT(I <sub>sat</sub> ) DC AMPS <sup>2</sup>	
			Typ.	Max.	Typ.	Max.
MMD-05CZ-R47MEV1L	0.47	6.2	12.2		16	



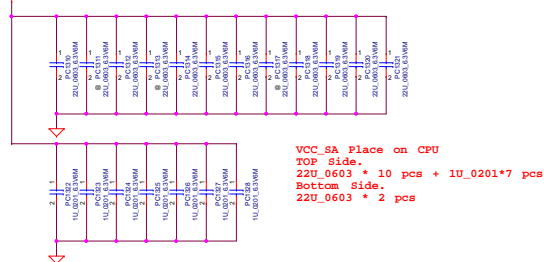
CPU\_Vcore controller(36.1), Drivers(36.2), Support component(36.3),  
GFX output CAP(36.5)



**+VCCGT**



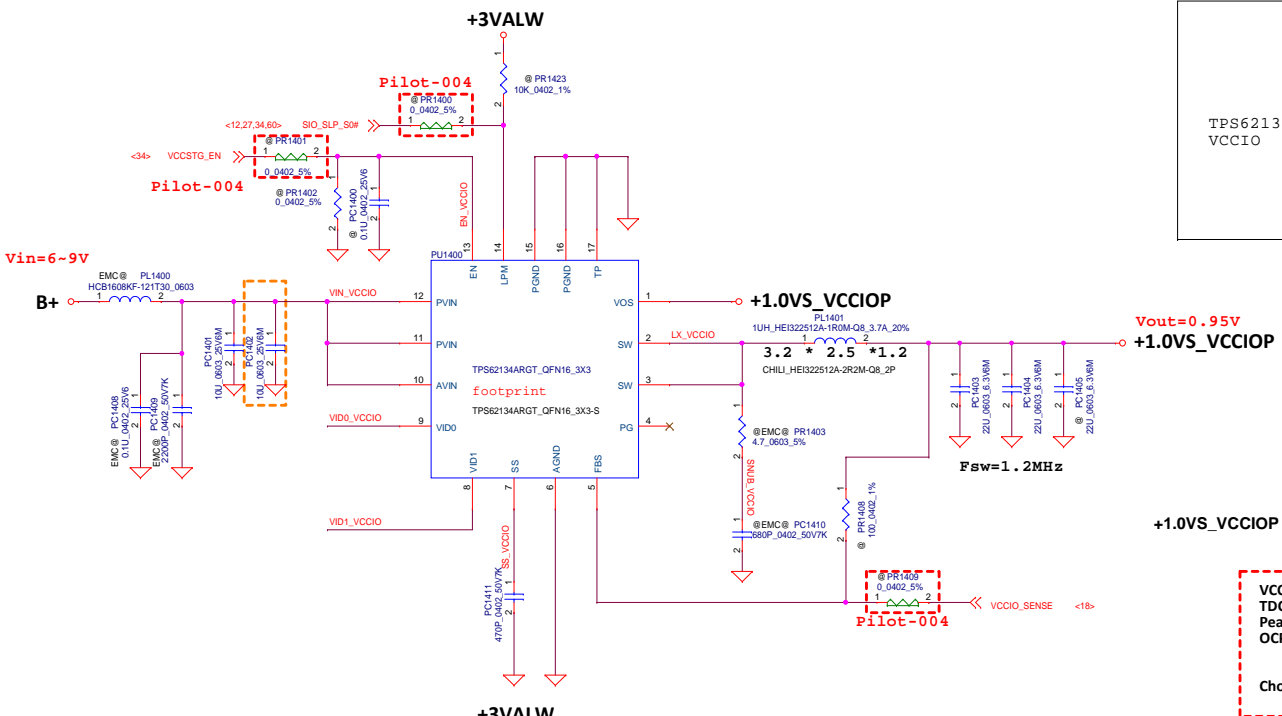
**+VCCSA**



VCC\_CORE output cap(36.4), VCC\_GT output cap(36.5), VCC\_SA output cap(36.6), VCC\_IAGT out cap(36.7)

Security Classification		Compal Secret Data		Title	
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	LPM	VID1	VID0	Vout
TPS62134A VCCIO	0	X	X	0.000 (LPM)
	1	0	0	0.850
	1	0	1	0.8750
	1	1	0	0.950
	1	1	1	0.975

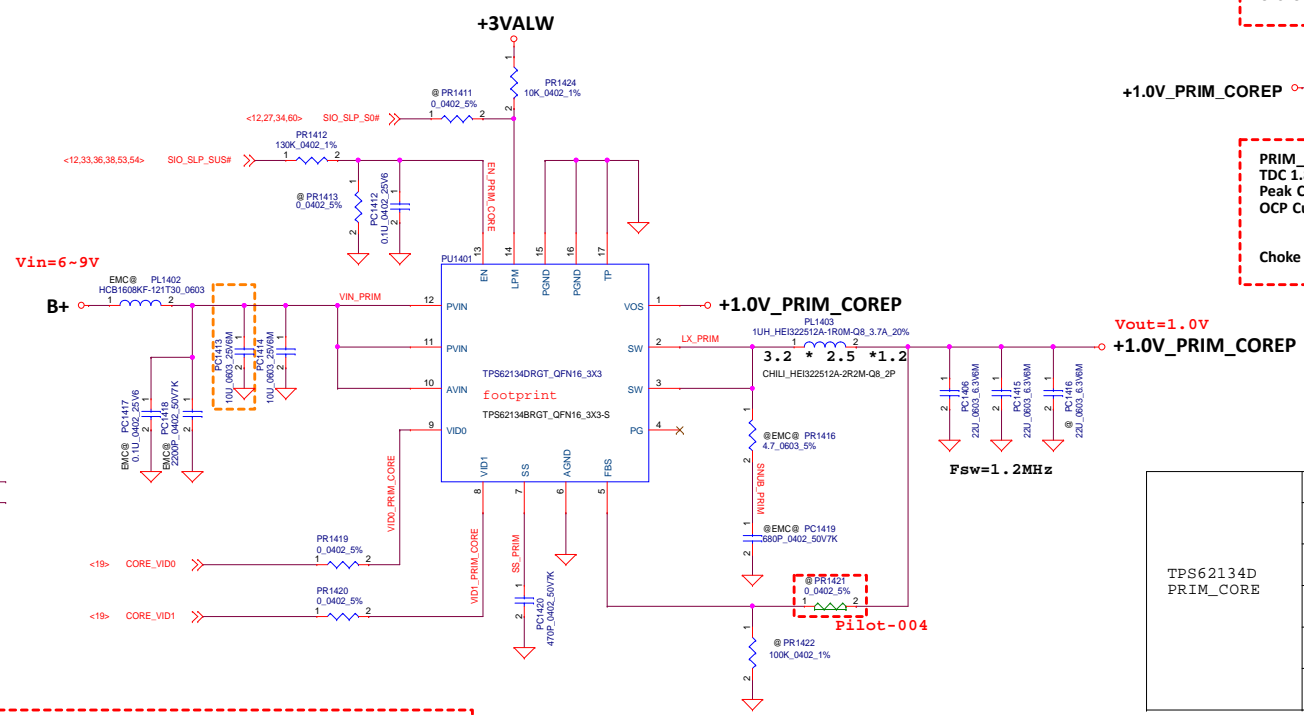


+1.0VS\_VCCIO

VCCIO  
TDC 2.2A  
Peak Current 3.1 A  
OCP Current 4.2 A Fix by IC  
MIN:3.6A  
MAX:4.9A  
Choke DCR 34.0mohm

+1.0V\_PRIM\_CORE

PRIM\_CORE  
TDC 1.8A  
Peak Current 2.6 A  
OCP Current 4.2 A Fix by IC  
MIN:3.6A  
MAX:4.9A  
Choke DCR 34.0mohm



+1.0V\_PRIM\_CORE

+1.0VS\_VCCIO controller(35.21), Support component(35.22)  
+1.0V\_PRIM\_CORE controller(35.23), Support component(35.24)

	LPM	VID1	VID0	Vout
TPS62134D PRIM_CORE	0	X	X	0.700 (LPM)
	1	0	0	0.850
	1	0	1	0.900
	1	1	0	0.950
	1	1	1	1.000

